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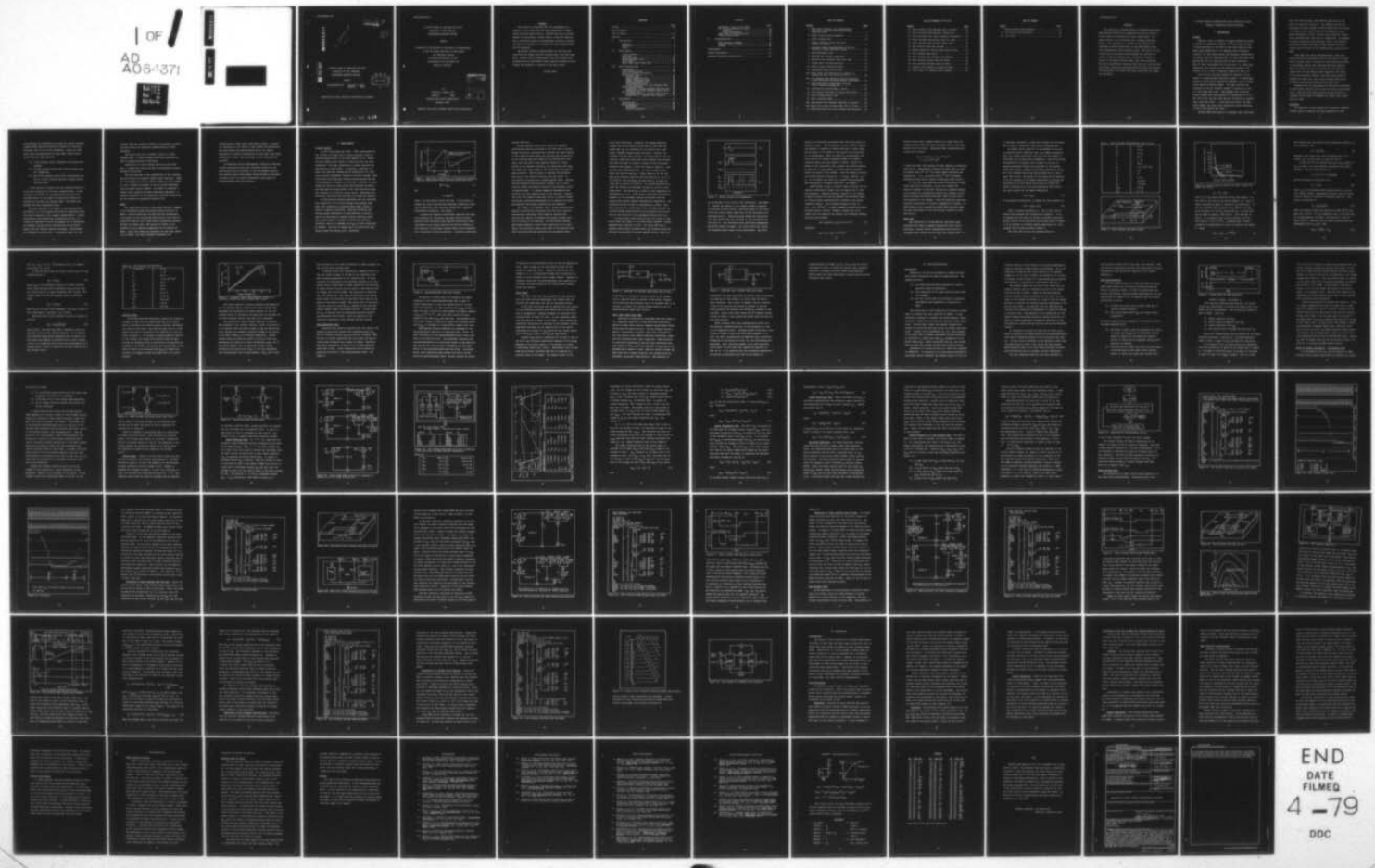

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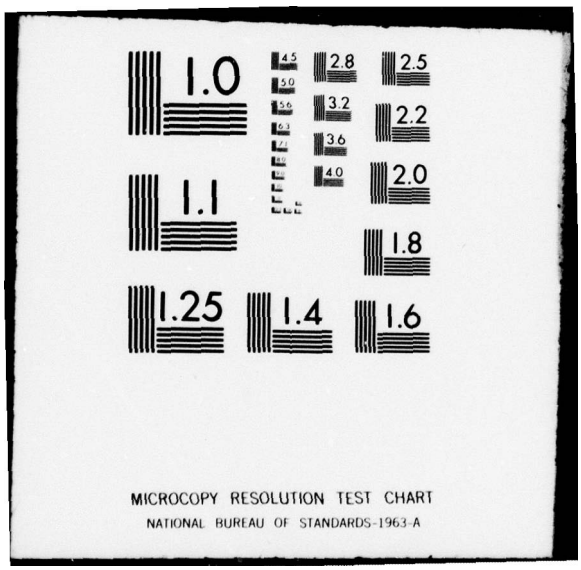
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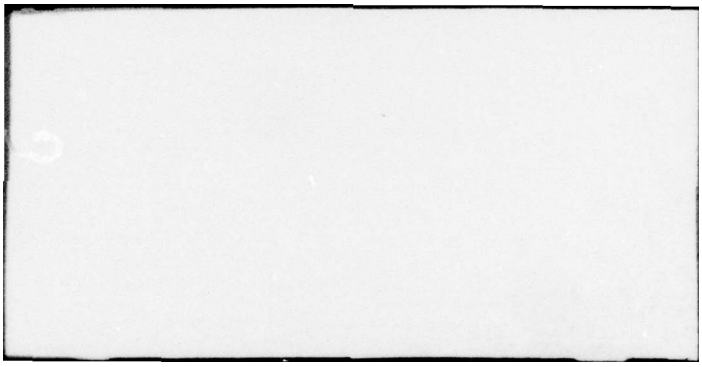

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A CIRCUIT MODEL TO SIMULATE THE LOGIC OPERATION OF FOUR TERMINAL TRANSFERRED ELECTRON DEVICES

THESIS

AFIT/GE/EE/78-38 Richard L. Roach
Captain USAF

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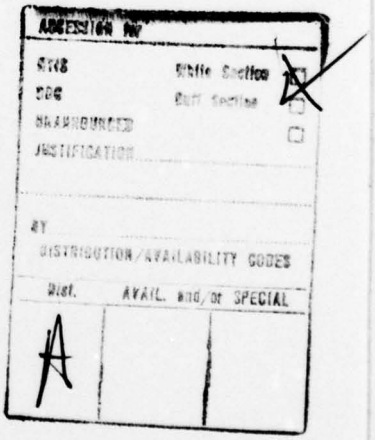
AFIT/GE/EE/78-38

A CIRCUIT MODEL TO SIMULATE THE LOGIC OPERATION OF FOUR TERMINAL TRANSFERRED ELECTRON DEVICES

THESIS

Presented to the Faculty of the School of Engineering
of the Air Force Institute of Technology
Air Training Command
in Partial Fulfillment of the
Requirements for the Degree of
Master of Science



by

Richard L. Roach, B.S.
Captain USAF
Graduate Electrical Engineering

December 1978

Preface

This thesis is concerned with the development of a computer circuit model for the logic simulation of Transferred Electron Logic Devices. Because this was an initial attempt at developing a circuit model, it was not expected that a definitive model be produced and, although a successful model was devised, it is hoped that other possibilities will be explored.

My special thanks to Captain Borky for his help and especially his always positive attitude about the work being done. Another word of thanks goes to my wife Mildred who, although did not understand a word, read and re-read my work, forward and backward, in search of the many errors.

Richard Roach

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Abstract

The operational characteristics of Transferred Electron Logic Devices (TELDs) were summarized and used to devise a circuit model for simulation of basic logic gates. The model consists of an oscillator and a voltage controlled switch. The oscillator is a series of RC circuits that discharge at rates proportional to the TELD domain formation, propagation, and extinction times. The switch is controlled by the oscillator and simulates the internal increase of device resistance due to electron transfer to states of decreased mobility under high field conditions. The model successfully simulated three and four terminal AND and OR gate operations and demonstrated the need for special considerations to be taken when logic operations with TELDs are performed.

A CIRCUIT MODEL TO SIMULATE THE LOGIC OPERATION OF FOUR TERMINAL TRANSFERRED ELECTRON DEVICES

I Introduction

Purpose

Design of logic to operate at gigabit speeds has become a subject of significant interest to the Air Force because of projected needs in the 1980 to 1985 time frame for high speed logic capability in (1) wideband direct frequency counters, (2) fast phase locked loop frequency synthesizers, (3) spread spectrum communications, (4) real-time radar data processing, and (5) high speed A/D and D/A converters. Many of these requirements can be met with 1 to 5 GHz logic capability, but others, such as frequency dividers, will require a 5 to 10 GHz, or greater, capability (Ref 1:1).

The Air Force has made feasibility studies in three areas: (1) Oxide Aligned Transistors (OATs); (2) Metal-Semiconductor Field Effect Transistors (MESFETs), and (3) Transferred Electron Devices (TEDs). OAT logic circuits are available in the LSI category capable of operating in the 1 to 2 GHz range (Ref 1:56). GaAs MESFETs with optimized circuit design have been operated at frequencies of up to 3 GHz (Ref 2:107) and may reach maximum frequencies of greater than 5 GHz (Ref 2:66). A relatively new device, the TED (Gunn diode), has shown logic capabilities while operating in the 10 GHz region (Ref 3:43).

Because TEDs show promise of extending logic operations

well into the GHz range, much work has been done in the study of logic-device physics. The highest priority has been given to basic studies of device fabrication in efforts to determine such characteristics as propagation delay, power dissipation, fan-in, fan-out, noise immunity, temperature considerations, and scale of integration. As progress in device fabrication has been made, some of the emphasis has shifted toward the study of logic systems with monostable devices because of the characteristic oscillation of TEDs.

Since TEDs have unique characteristics, other than their distinctive oscillation, which allow them to be operated in several modes, a variety of unit structures capable of performing complex logic functions has been proposed. These structures include such devices as n-bit parallel adders (Ref 4:1) and dynamic shift registers (Ref 5:926). It has been proposed, however, that basic logic gates be produced in order that logic circuit design rules may be optimized using TED monostable devices (Ref 6:26).

Together with the development of fabrication techniques of basic gates, efforts must be made to develop logic design tools. One such tool which would be of great value is a computer circuit model to simulate the unique logic operation of a TED.

Objective

The objective of this thesis was to develop a computer circuit model to simulate the logic operation of a TED

and determine the feasibility of using the circuit analysis program ASPEC (Advanced Simulation Program for Electronic Circuits) (Ref 7:A-1) in the simulation. There are three basic logic configurations for logic TEDs, TELDs (Transferred Electron Logic Devices):

(1) a two terminal device comprised of an anode and a cathode,

(2) a three terminal device which has a Schottky gate for triggering,

(3) and a four terminal device which incorporates the use of a three terminal TELD and a domain detecting electrode.

It was decided to simulate the four terminal TELD as it is the most versatile of the three configurations. It was necessary to simulate all configurations since the four terminal device is the product of sequential addition of contacts to the basic two terminal TELD. The effort was divided into four progressive steps.

The first step was to determine if the characteristic oscillation of a two terminal TELD could be duplicated using the circuit elements in the computer program ASPEC. Certain problems were encountered that necessitated the use of a "black box" approach in which the emphasis is on replicating the terminal voltage-current relationships of the device rather than the internal physical processes. The problems are discussed in section III. A successful model of a two

terminal TELD was created in which it is possible to establish and control the essential characteristics of TELD operation.

The second step was to produce a model of a three terminal TELD. A three terminal device was simulated and used to produce AND and OR functions.

Simulation of a four terminal device was the third step. A model was created and used to successfully produce AND and OR functions.

The last step was to use combinations of four terminal AND and OR gates to simulate complex logic functions. ASPEC has the capability to use a circuit system as a macro wherein, once a system is defined, it may be called repeatedly like any ASPEC circuit element. An attempt to simulate a dynamic shift register was made using macro AND gates. A complete discussion of the simulation, problems encountered, and the results is presented in section III.

Scope

The remaining sections of this report include a summary of the background theory and present state-of-the-art of TELDs, a section detailing the work that was accomplished, a discussion of the conclusions which can be drawn from the simulation results, and a final section presenting recommendations for future work. The section on theory is not intended to be an indepth presentation on the physics of TELDs. Since this thesis is concerned with the logic operation of TELDs, only that information necessary for

understanding of TELD logic conditions is given. A wealth of information on the theory of Gunn diodes and Transferred Electron Devices has been published since J.B. Gunn's observation of current oscillations in GaAs under high field conditions in 1963, and references to the literature are provided.

An additional author bibliography listing all reference sources encountered during the literature search but not specifically used is included in the bibliography section. This special author bibliography should provide an excellent reference source for anyone interested in any aspect of Transferred Electron Logic Devices.

II Basic Theory

A Short History

In 1827 Georg Simon Ohm (1789 - 1854) established his law in which he stated that a current through a solid is directly proportional to the field applied to it. Metals are well behaved with respect to Ohm's Law, but not semiconductors. The high conductivity of metals prevents the application of high fields. In addition, electrons in a metal have high mean energy and the application of a high field produces negligible increase in electron energy. High conductivity and high mean electron energy account for the strict adherence of metals to Ohm's Law. Electrons in semiconductors have much less energy than electrons in metals and high applied fields produce "hot" electrons which alter the occupancy of electronic energy states. Semiconductors, therefore, obey Ohm's Law only when low fields are applied.

In 1948 William Shockley speculated that the deviation from linearity in the current-voltage relationship under high field conditions in semiconductors might produce a region of negative resistance. Shockley theorized that because energy dissipation in semiconductors is mainly a result of scattering by thermal lattice vibrations where only a small amount of energy is removed per electron collision, there is a maximum rate P_{max} at which energy can be removed. The rate of energy input to an electron, eE_v, cannot exceed the removal rate. Therefore,

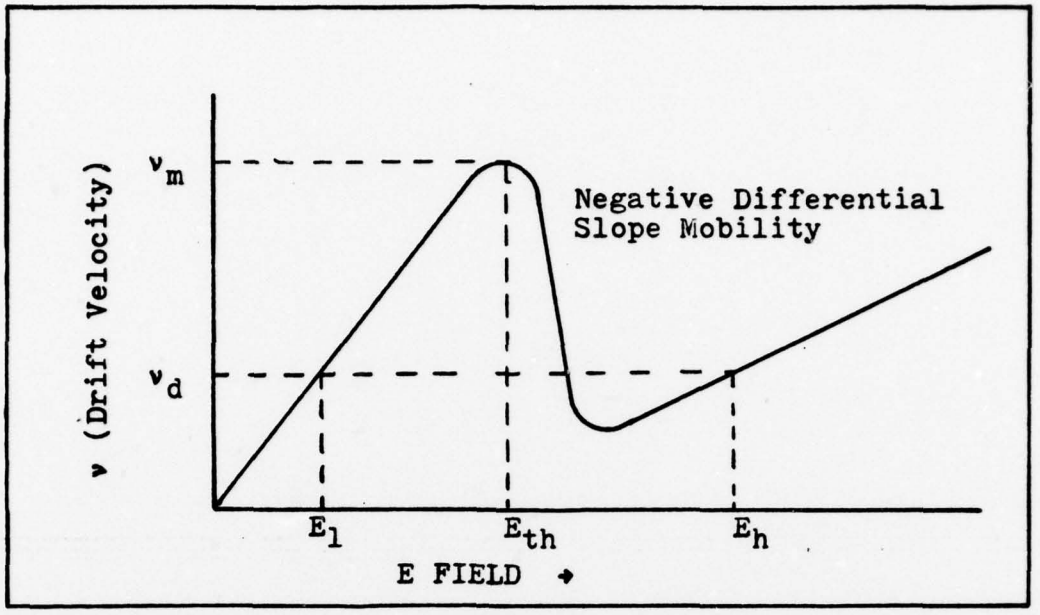


Figure 1. High field condition in a semiconductor producing a negative differential slope mobility, dv/dE (Ref 8:7).

$$eEv \leq P_{max} \tag{1}$$

and

$$v \leq P_{max}/eE \tag{2}$$

where v is the electron drift velocity. As the field increases the drift velocity must decrease, producing a negative differential slope mobility (dv/dE) and a negative differential resistance. See Figure 1.

A search for negative differential mobility (and negative differential resistance) was made without success. Shockley later speculated that negative differential mobility based on his theory would not be detected because of the injection of additional carriers which would compensate for a reduction in carrier mobility. A positive conductance

results (Ref 8:4).

Another approach used in the search for negative differential mobility was based on the idea that if enough energy is applied, electrons will populate the upper regions of the conduction band where the electron mass is negative. As the electron mass goes negative the electron will slow down, stop, and move in the opposite direction. While moving in the opposite direction, the electrons (with negative mass) will lose energy to the field until the mass is again positive. When the mass is positive the electrons will move in the orginal direction with the field. An oscillation is produced by a steady applied field. Scattering and avalanche multiplication, however, act to limit electron energy and prevent electrons from reaching a state of negative mass. H. Kroemer suggested experiments with holes as they have negative mass at low energies. Because the holes with negative mass must travel in certain crystal directions, scattering mechanisms act to disperse the holes and negative differential mobility was not observed.

B.K. Ridley, T.B. Watkins, and C. Hilsum realized that negative differential resistance (NDR) and thus, negative differential conductance (NDC) might be observed when carriers are induced to transfer from states of high mobility to states of low mobility. For the Ridley, Watkins, and Hilsum mechanism to work three conditions must be met. First, two electronic states must exist in the material such that electrons with high mobilities are maintained under

high field conditions. Secondly, the energy separation between the two electronic states must be less than the energy gap, E_g, or ionization of the lattice will occur before transfer between states can start. Thirdly, the transfer from the high mobility, low field state to the low mobility, high field state must occur rapidly with increasing field in order to produce a region in the v-E characteristics (see Figure 1) where the slope is negative. GaAs has all three characteristics. It has a central valley where the electron mass $m_1 = .072m_o$ (where m_o is the rest mass of an electron) and the electron mobility μ_1 is 8.5 x 10^3 $cm^2/V\text{-}S$, plus secondary valleys where m_2 is equal to $.36m_o$ and μ_2 equals 100 $cm^2/V\text{-}S$. The energy separation between the central and secondary valleys is .36 eV at room temperature. The energy gap of GaAs at room temperature is approximately 1.4 eV. Under proper conditions the electron transfer to the secondary valleys occurs such that the crystal does exhibit negative differential conductance. The threshold for NDC in GaAs is approximately 3 kV/cm. Once the electrons have transferred to the secondary valleys the current-voltage characteristics are determined by the mobility of the electrons in the secondary valleys (Ref 8:6).

A crystal whose field velocity lies in a region of negative slope (see Figure 1) is electrically unstable. Ridley analyzed this condition in 1963. He stated that when a crystal such as GaAs is biased above the threshold value for NDC and a fluctuation of carrier density occurs, there will

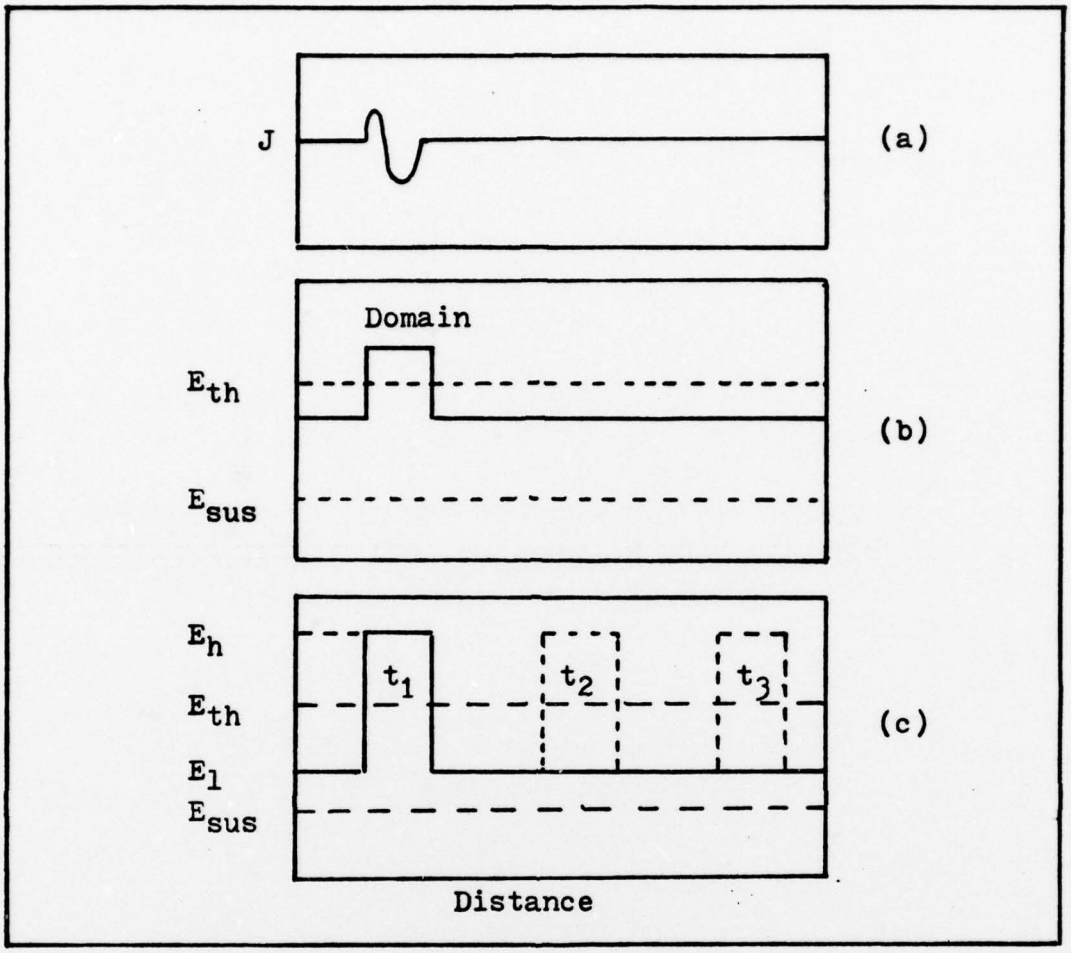


Figure 2. Domain creation and propagation.

be an increase in the field at the fluctuation. See Figure 2. Because the crystal is in a region of NDC a reduction in electron velocity occurs. Electrons ahead of the fluctuation will travel faster than those in the fluctuation and move away from it. Those electrons behind the fluctuation will move faster than the electrons in the fluctuation and pile into it. The fluctuation will grow while propagating until the crystal is stable. The field inside the crystal is everywhere equal except in the fluctuation. The field

inside the fluctuation is greater than the field inside the neutral crystal. The fluctuation is now a stable "domain," and because it consists of mobile electrons it moves under the influence of the field to the positive electrode where it is extinguished. When the domain is extinguished, the field inside the crystal increases toward its original threshold value and a new domain is formed. Before the growth of the fluctuation into a domain the current density is given by $J = n_o e v_m$ where v_m is the electron velocity before the growth of the domain. After the domain is formed the current density is given by $J = n_o e v_d$. Because $v_m > v_d$ it is evident that there is a current drop associated with the growth of a domain (Ref 8:6). See Figure 1.

There exists in GaAs a critical range of values for the carrier concentration length ($n_o \ell$) if domains are to form and propagate. Complete numerical analysis of the domain formation process was done by McCumber and Chynoweth based on velocity-field characteristics, diffusion, and energy transport effects. This analysis obtained a value of $n_o \ell = .76 \times 10^{11} cm^{-2}$. A simple argument proposed by Kroemer produced similar results. Because a domain may not be longer than the length of the device, the difference between E_h and E_l must satisfy

$$\Delta E < n_o \ell e / \epsilon \epsilon_o = n_o \ell \times 1.6 \times 10^{-7} \qquad (3)$$

therefore,

$$n_o \ell > \Delta E \times .625 \times 10^7 \ cm^{-2}. \qquad (4)$$

Kroemer stated that a domain should be at least twice the threshold field value and that the domain must be very much shorter than the device. Weighting these considerations at a value of 4 yields:

$$n_o \ell \cong 4(3 \text{ kV}) \times .625 \times 10^7 \text{ cm}^{-2}$$
$$\cong .75 \times 10^{11} \text{ cm}^{-2}$$

a value very near that required by more rigorous calculations (Ref 8:114). Experimental evidence has shown that $n_o \ell$ must be greater than 10^{13} cm^{-2} for proper domain formation and propagation. If n_o is greater than 10^{17} cm^{-3} avalanche breakdown occurs and the device is destroyed (Ref 9:1435).

In 1963 J.B. Gunn observed current oscillations in GaAs under high field conditions. He did not consider the electron transfer to satellite valleys as a possible explanation because the temperature required for transfer as estimated by Ridley and Watkins was about 4000^o K, well above that measured in his samples. Gunn overlooked the much more accurate calculations of electron temperature by Hilsum. In 1965 Hutson, et al, removed all doubts that electron transfer was responsible for the oscillations observed by Gunn (Ref 8:7-9).

Basic TED

The possibility of using TEDs for high speed logic functions was widely recognized immediately after Gunn's discovery. Several device configurations which will be discussed have evolved from the basic two terminal TED. It

is important, therefore, to gain more insight into the basic TED in order to understand other device configurations.

To predict device behavior it is necessary to be able to determine domain formation time, T_{df}; domain propagation time, T_{wd}; domain extinction time, T_{de}; and the change in resistance, ΔR, during domain propagation. From the previous discussions it is apparent that a domain is an area of charge accumulated through the resistance of the crystal. Using this concept a simple and accurate description of T_{df} for a two terminal device has been proposed by H.L. Hartnagel (Ref 10:21). The growth of the domain may be described as the charging of the domain capacitance C_d through the resistance R_o of the crystal which does not contain the domain (essentially the low field resistance (Ref 8:262)). One time constant for the domain charging is

$$1\ TC = R_o C_d. \tag{5}$$

If an external resistance R_1 is added, the time constant is

$$1\ TC = C_d(R_o + R_1). \tag{6}$$

Table I presents published data (Ref 11:510) from an actual three terminal TED illustrated in Figure 3. If it is assumed that the point of carrier fluctuation described earlier occurs at the same point as the gate shown in Figure 3, it is possible to estimate domain capacitance for a two terminal device using the data in Table I.

The total bias for the two terminal device is

Table I. Three Terminal TED Parameters (Ref 11:510).

ℓ_t	85 μm
ℓ_g	12 μm
ℓ_c	15 μm
W	58 μm
d	5 μm
R_o	305 Ω
n_o	1.2×10^{16} cm^{-3}
k_o	.52
a_o	17
t_w	1 ns
V_a	46 Volts
V_g	-4 Volts
I_{tho}	104 mA
I_{og}	40 mA

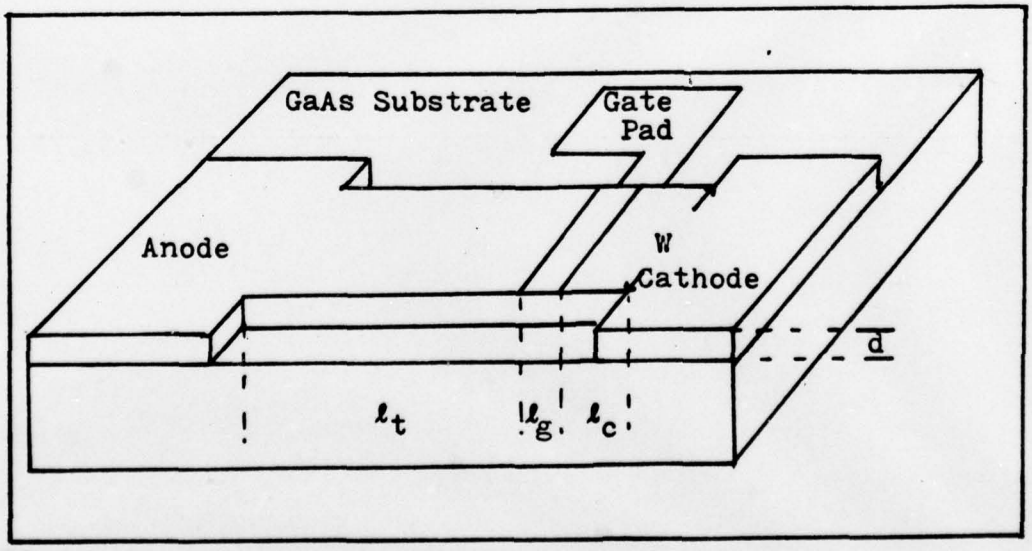


Figure 3. Three terminal TED (Ref 11:506).

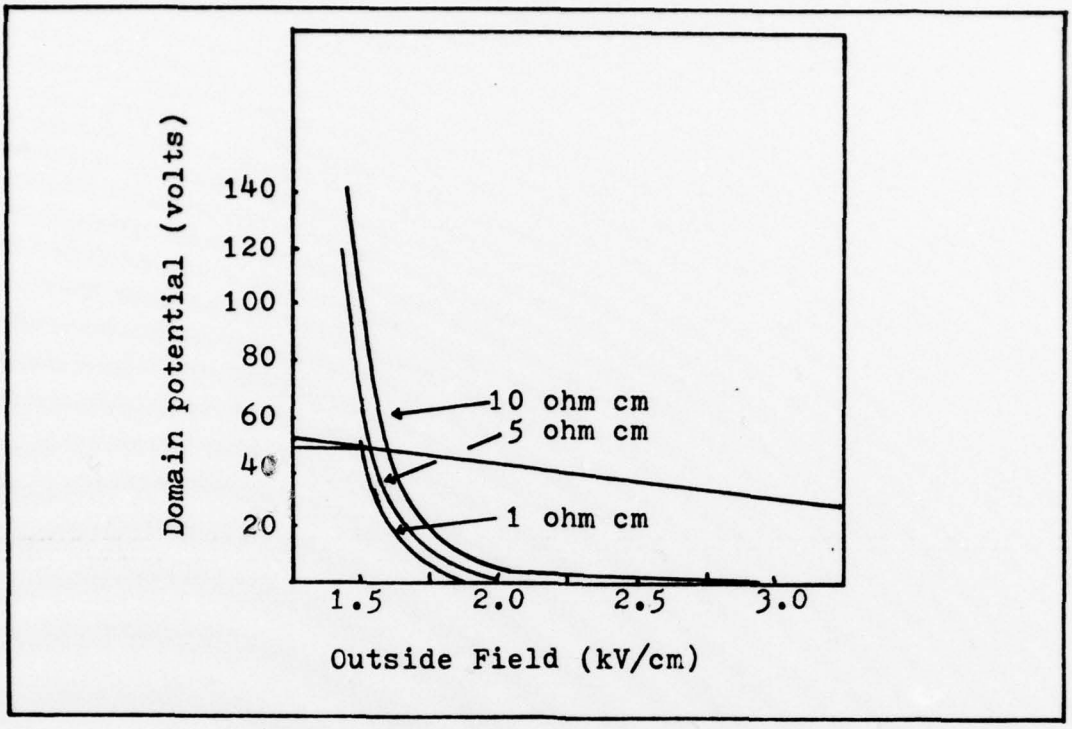


Figure 4. Domain potential versus the field outside the domain (Ref 8:124).

$$V_{th} = V_d + E_1 \ell_t \tag{7}$$

where V_d is the domain potential and E_1 (see Figure 1) is the field in the rest of the active channel, ℓ_t. Prior to domain charging V_d equals 0, therefore V_{th} equals $E_1 \ell_t$. If all the potential were absorbed by the domain, then $E_1 \ell_t$ would be equal to 0 and V_{th} would equal V_d. A "load line" may be drawn on Figure 4 (Ref 8:124). From the data in Table I it is apparent that 3.4 Ω cm GaAs was used (R_o = 305 Ω and $\ell_t = 112 \times 10^{-4}$ cm). Interpolating, a domain potential of approximately 45 Volts is obtained from Figure 4. Using

$$V(t) = V_d(1 - e^{-t/R_o C_d}) \tag{8}$$

and assuming that the domain will be completely charged in 5 time constants, then

$$C_d = T_{df}/5R_o. \tag{9}$$

Hartnagel also states that the discharging time of the domain, T_{de}, is about equal to T_{df} (Ref 10:21).

If the width of the current drop pulse (t_w in Table I) T_{wd} is known, it is now possible to complete this simple analysis. The low field mobility is

$$\mu_o = \ell(t + g + c)/n_o e R_o W d \tag{10}$$

and the frequency of operation f_o is

$$f_o = v_d/\ell_t \tag{11}$$

where v_d is the saturated drift velocity and ℓ_t is the active channel length. Measurements indicate that the domain velocity varies in proportion to material mobility. Frequency of operation is

$$f_o = v_d \mu_o/\ell_t 8500 \tag{12}$$

where the maximum theoretical mobility is 8500 $cm^2/V\text{-}S$ for GaAs (Ref 12:273). If v_d is assumed to be 1×10^7 cm/s then f_o is approximately .9134 GHz. The period ($T = 1/f$) is about 1094 ps. Assuming that the domain charging time and discharging time are equal, then

$$2T_{df} = 1094ps - T_{wd} \tag{13}$$

and $T_{df} = T_{de} = 47$ ps. From equation (9) C_d is approximately equal to .03 pF.

It has been shown that the output current i_{oa} for a two terminal device is

$$i_{oa} = k_o I_{tho} \tag{14}$$

where I_{tho} is the threshold current for a three terminal device with the same active dimensions and k_o is the relative field drop due to domain formation (Ref 11:507). The current output for the two terminal device is 54.08 mA. Using

$$R_{hf} = V_{th}/i_{oa} \tag{15}$$

where R_{hf} is the high field resistance, then R_{hf} is equal to 865 Ω resulting in a ΔR ($R_{hf} - R_o$) of 560 Ω.

Threshold power (power required to produce a domain) is given by

$$P_{th} = en_o\mu_o E_{th}^2 \ell_t dW \tag{16}$$

(Ref 9:1436). The data from Table I indicate a power requirement of 89.9 mW for domain formation. It is apparent that tradeoffs among device parameters must be made to reduce power requirements of switching device power consumption is to be compatible with total power requirements for a complex system. Table II summarizes the data obtained for a two terminal device.

Table II. Two Terminal TED Parameters.

ℓ (active)	85 μm
d	5 μm
W	58 μm
n_o	1.6×10^{16} cm^{-2}
R_o	305 Ω
ΔR	560 Ω
R_{hf}	865 Ω
V_{th}	46.75 V
i_{oa}	54.08 mA
ΔI	99.23 mA
C_d	.03 pF
P_{th}	89.9 mW

Depletion Mode

In the TED described previously a domain was created in a sample of GaAs that was biased above E_{th} at the point where a fluctuation of carrier density occurred, increasing the field at that point. The field at some point on a TED channel may also be increased by the addition of a gate as shown in Figure 3. If the gate is biased negative relative to the channel, the channel will deplete under the gate causing the threshold value of the field to be exceeded and a domain to be formed. As with the two terminal TED, if the field is above the sustaining field E_{sus} the domain will continue to propagate toward the anode where it is extinguished.

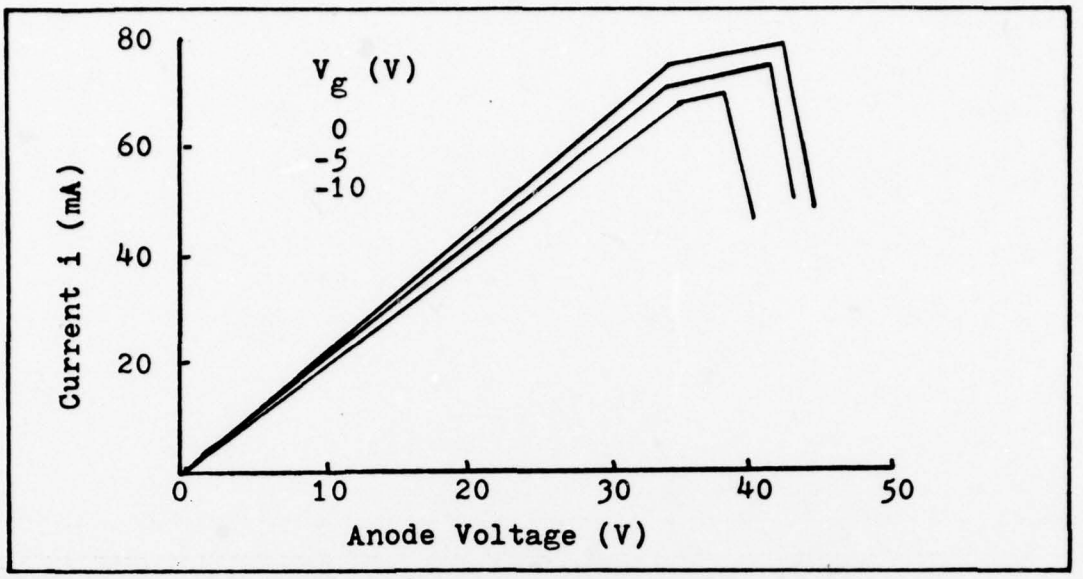


Figure 5. Piecewise linear representation of NDC as a function of anode and gate voltage (Ref 11:504).

The simple analysis of device parameters performed for the two terminal TED is valid for the three terminal TED (assuming the fluctuation in carrier density for the two terminal device is located at the same point as the gate for the three terminal device) and will not be repeated.

Two points about three terminal TEDs are of interest when compared to two terminal devices. First, from Figure 5 it is apparent that the anode voltage V_a may be reduced and still produce the necessary threshold voltage in the device if the gate voltage V_g is increased negatively. Second, because there are practical limits to V_g due to such considerations as reduction of power dissipation, pinch off of the active channel, and the magnitude of gate voltage available from any previous stage, it has been determined that optimum anode bias is approximately $.95V_{th}$ (Ref 13:30).

This accounts for the slight difference in anode voltages for the two and three terminal TEDs.

A problem exists with sequentially triggered devices in that the output voltage of one TED is not compatible with gate voltage requirements of the follow-on TED. To avoid inclusion of complicated level shifting networks in an integrated circuit using TEDs, a simple capacitive electrode may be added between the gate and the anode of each TED and used to trigger any follow-on TEDs. The electrode is insulated from the channel by a thin layer of SiO_2 and as the domain passes under the electrode the potential there drops by the amount of the domain voltage. The pulse width of the potential drop under the electrode T_{el} depends on the electrode length, domain length, and domain velocity. A pulse width for T_{el} of several tens of picoseconds has been obtained experimentally (Ref 14:408). With the addition of the capacitive electrode, a four terminal TED has evolved.

Quasienhancement Mode

Depletion mode operation requires that the field in the channel be maintained between some sustaining field E_{sus} and the threshold voltage E_{th} with the gate floating. When the gate is biased negatively, the field under the gate is raised above threshold and a domain is formed. Depletion mode power dissipation is about .8 to .9 times threshold power (Ref 15:262). Power dissipation can be reduced by operating the device in the Quasienhancement Mode. See Figure 6.

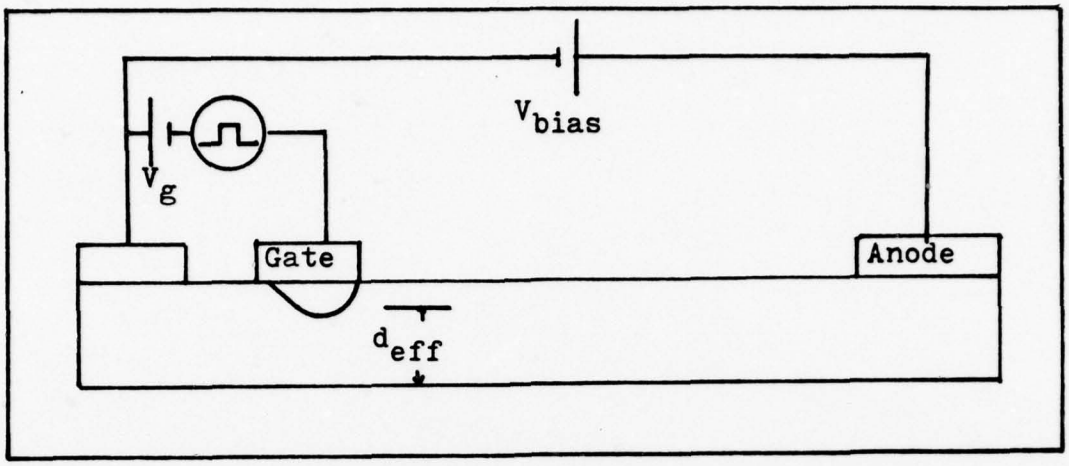


Figure 6. Quasienhancement mode (Ref 15:262).

The device is biased above the threshold for domain formation in the quasienhancement mode and the gate is biased (negatively) so that the channel below it is more than half depleted. In this condition the $n_o d_{eff}$ product under the gate is below the value needed for domain creation ($n_o d_{eff} \geq 10^{12}$ cm^{-2}). Thus the field outside the gate region is well above E_{sus} and below E_{th}. By applying a positive gate voltage the depletion region will decrease allowing $n_o d_{eff}$ to increase to a value where a domain will form.

Experimental evidence indicates two advantage of the quasienhancement mode over the depletion mode. First, the power dissipation in the quasienhancement mode is much less than in the depletion mode. One experiment indicated that the power dissipation of a particular device in the depletion mode was 225 mW while the power dissipation for the same device in the quasienhancement mode was 45 mW. In another device power dissipation was reduced from 180 to 120 mW using the quasienhancement mode. Second, because the device

is operated on the saturated portion of the I/V characteristics, small changes in the bias supply voltage do not change the operating point. Depletion mode devices are biased at .9 to .95 threshold voltage and fluctuations in supply or noise voltages could trigger domains. Research is presently being done on quasienhancement mode operation to determine the exact causes for the reduced power requirements (Ref 15:263).

Other Modes

Two other ideas have been proposed for TED operation, each with some specific advantages, but because they are relative new ideas they will only be discussed briefly.

It has been discovered that as domains form they spread in the transverse direction much faster than in the direction of propagation. Domains propagate at saturated drift velocity which is about 10^7 cm/s. In the transverse direction the velocity is about 7×10^7 cm/s. Also, because the transverse velocity is not affected by the external circuit, high-speed switching can be expected even if the device dimensions are reduced to the limits for full domain growth ($\ell_t = 10^{13}/n_o$ cm and $d = 10^{12}/n_o$ cm) (Ref 16:27).

Another unique mode of operation for the TED is that if the drift and diffusion currents are balanced at the doping gradient of the anode contact, it is possible to produce a stationary domain (Ref 17:681). Experimental work in this area has produced a bistable TED that is triggered by a positive pulse at the anode. The domain travels to the

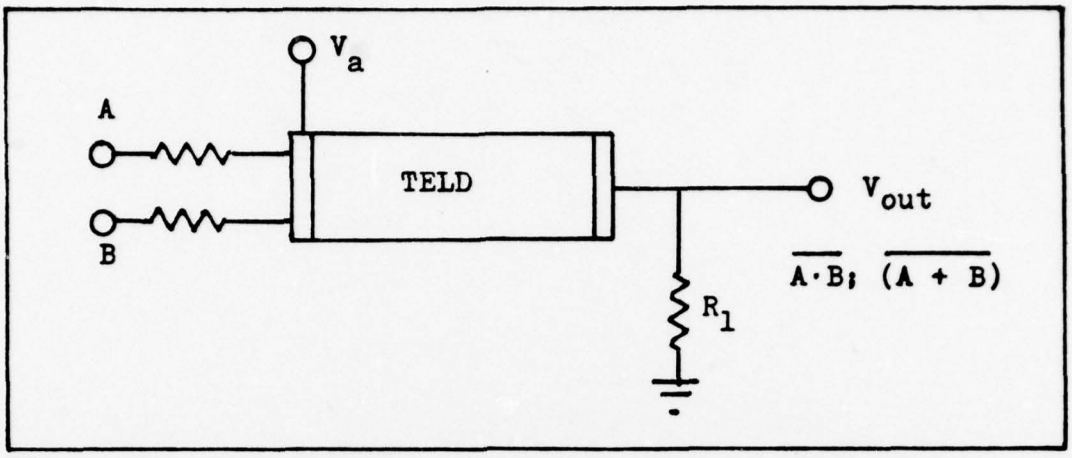


Figure 7. NAND-NOR two terminal logic gate (Ref 19:335).

anode where it is held by a groove etched in the channel until a negative pulse is applied to the anode. Subnanosecond switching was achieved, and it is believed that it is possible to produce the trapped domain action by use of Schottky-barrier gates (Ref 18:361).

Basic Logic Gates Using TEDs

Logic gate configurations using TEDs have been based on the triggering capability of some additional externally applied voltage source and are commonly called TELDs (Transferred Electron Logic Devices). For two terminal devices, Figure 7 represents a universal logic gate configuration that may perform either NAND or NOR (see Conclusions, Logic Function Considerations) logic operations. NAND operation is achieved by adjusting V_a and the input resistances such that inputs to both A and B are required to cause E_{th} to be exceeded and a domain to form. When the current through the TELD drops due to domain formation, the voltage across R_1 decreases, producing a NAND function. NOR operation is

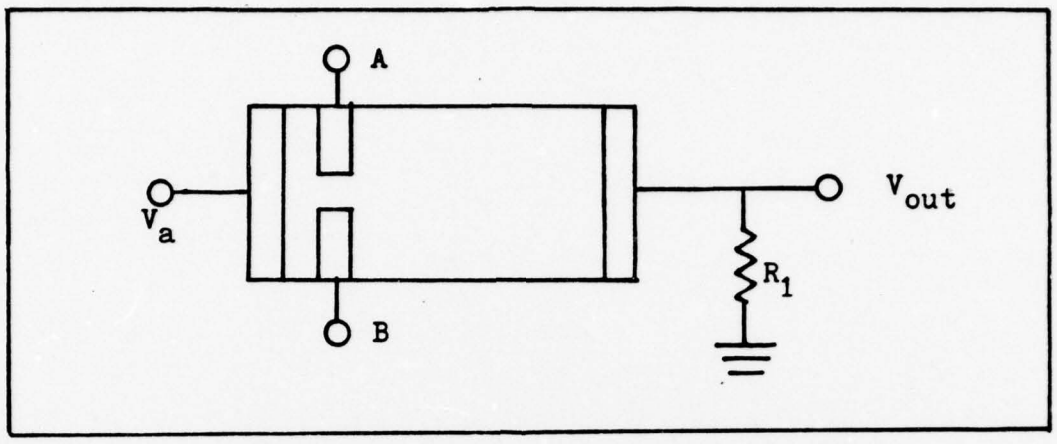


Figure 8. NAND-NOR three terminal TELD logic gate.

essentially the same except that V_a and the input resistances are adjusted so that either A or B will bias the device above threshold. The circuit in Figure 7 can be converted to AND or OR operation by placing R_1 between V_a and the TELD, grounding the cathode, and taking V_{out} between R_1 and the TELD. Actual logic gates using the two terminal configuration of Figure 7 were tested and proven valid as early as 1970 (Ref 19:335).

Three terminal TELD logic configurations differ from two terminal configurations only in the placement and type of the triggering source. Although several variations on the circuit in Figure 8 (Ref 3:30) have been proposed, it is still the basic configuration for NAND-NOR logic operations. Triggering is introduced at A and, or, B by Schottky-barrier gate pads. Logic operation depends on how much depletion occurs under the gate pads when signals are applied to A and, or, B. It is apparent from the discussion presented in the section on depletion mode that as the number of

triggering gates increases V_g, V_a, and n_o must be tightly controlled in order to obtain the desired logic operation (Ref 3:37), although multi-gate TELDs using Schottky-barrier gates have been successfully tested without serious difficulty (Ref 5:927).

III TELD Modeling Study

Assumptions

Modeling of the circuit parameters of TELDs required that certain assumptions be made for simplification. The assumptions were:

(1) only TELD characteristics required for circuit operation would be duplicated,

(2) only simulation of the gated depletion mode would be attempted,

(3) and the circuit model would attempt to duplicate experimental data presented in literature on TELDs.

The stated goal of this thesis was to develop a circuit model to simulate the logic operation of TELDs. It was, therefore, necessary to consider only those physical characteristics of TELDs that are directly related to logic operations. Schottky gate, anode, and cathode voltages were treated as conditions that must be met for proper TELD operation. Internal device parameters (n_o, etc.) were assumed to be correct and to produce predictable results (frequency of operation f_o, domain rise time T_{df}, propagation of the mature domain T_{wd}, domain extinction time T_{de}, and current drop ΔI) when the external contacts were properly biased.

Assumption (1) allows the use of a "black box" approach to simulation. In simulation of a large system comprised of individual circuit elements, the primary concern is with the

external effects of each element on the system expressed in terms of terminal voltage-current relationships. It is not necessary to simulate the actual physics of the element. Indeed, as in the case of TELDs, the simulation of the actual physics of each element of a large system may be prohibitive because of computational requirements (Ref 20:1).

The primary reason for the use of the "black box" approach, however, was the constraints placed on the simulation by the use of ASPEC. ASPEC was the most advanced circuit analysis program available for the study, but because of the unusual attributes of a TELD it does not appear possible to simulate the internal physical mechanisms of the device using ASPEC. The approach used for TELD modeling involves the charging and discharging of a capacitor through a resistive load. This approach is not unrealistic as the domain formed during TELD operation consists partially of a layer of charge accumulated through the resistance of the semiconductor crystal and any external load as was described earlier.

As indicated in section II there are two basic gated modes of operation for TELDs (depletion and quasienhancement) with several different methods of use (transverse and static). Of the choices available, it was decided to model only the gated depletion mode. This choice was made because gated depletion mode is the most widely discussed in available publications and is, perhaps, the best understood.

The last assumption made was that data obtained in

publications on TELDs will be the basis for modeling. Time and facility limitations precluded the possibility of actual fabrication of any device for comparison with computer simulation.

TELD Characteristics

The one characteristic of a TELD that makes it unique among logic devices is its current oscillation when the device is properly biased. In order to precipitate TELD current oscillation, certain biasing conditions must be met. From section II (Figure 2) it is apparent that for current oscillation to occur:

(1) E inside the device must be grater than E_{th} to initiate domain formation,
(2) and E must remain above E_{sus} for proper domain propagation.

The above conditions may be applied to the device in one of two ways (possibly both):

(1) The anode voltage V_a may be maintained such that E is always above E_{sus}, and an additional voltage source is applied to the anode (two terminal device) in order that E is greater than E_{th} when operation is desired.
(2) The anode may be biased such that E is above E_{sus}. A Schottky gate is then added (three terminal device) in order that proper gate voltage will

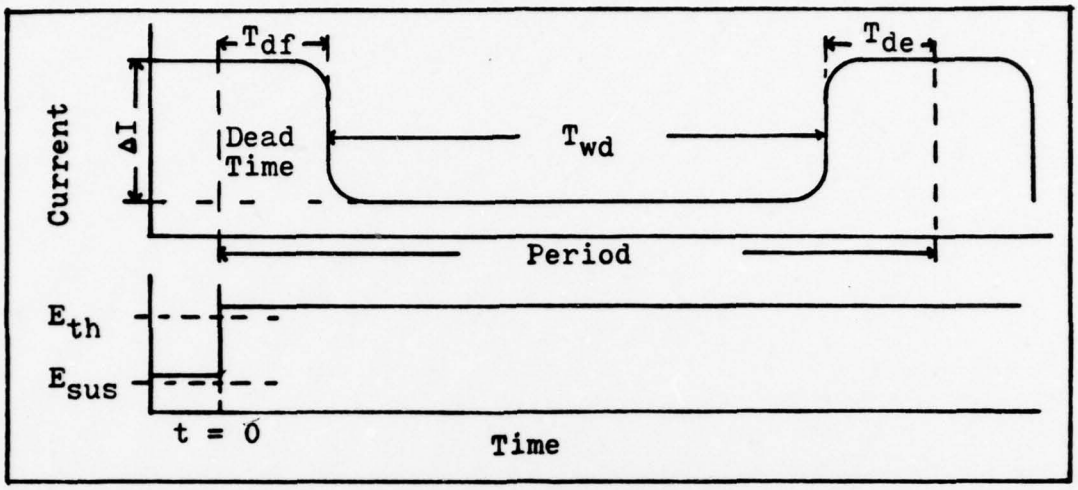


Figure 9. Timing chart for TELD operation.

produce a domain. See Figure 3.

After biasing conditions have been met, the current through the TELD begins to oscillate as domains form, propagate, and are extinguished. Four oscillation conditions must be known. They are:

(1) domain formation time T_{df},

(2) mature domain propagation time T_{wd},

(3) domain extinction time T_{de},

(4) and current drop ΔI through the TELD after T_{df}.

These four characteristics may be obtained by the simple procedure described in section II. The TELD parameters shown in Table I (page 14) were the basis for simulation.

It is helpful to put the TELD oscillation characteristics into perspective by means of the timing chart in Figure 9. A voltage of sufficient value is applied (at the anode or gate) at time 0 to trigger a domain. There is a dead

time in which the domain is forming and propagating but the current remains essentially constant (Ref 8:266). At the end of the dead time the current through the device drops rapidly as a direct function of the magnitude of the trigger voltage (Ref 20:36-37). Once the current drops, it remains at its lowest level while the domain propagates the remaining distance to the anode. As the domain contacts and begins to run into the anode, the current in the device rises to its original level. Once the first domain is extinguished the entire process begins again if the external bias conditions remain unchanged.

Several observations can be made from Figure 9. First, the domain triggering pulse must be longer than the dead time if a domain is to be set in motion. Second, if the current drop after the dead time is very short in relation to T_{wd} (which seems to be the case based on a survey of available data), T_{df} may be taken as the time for I to drop to its lowest level. A pulse travel time through a system of sequentially triggered TELDs could, therefore, be as short as the sum of all the domain formation times neglecting external circuit capacitance. This is not true for a four terminal device as will be demonstrated later. Lastly, T_{wd} must be greater than T_{df} for any follow-on device if a pulse is to propagate through several devices.

Model of Current Oscillation - Two Terminal TELD

An investigation into the circuit elements of ASPEC produced three possible approaches for modeling the current

oscillation of TELDs:

(1) an oscillating current source with the proper time parameters in series with a resistor,
(2) a FET model with a time varying transconductance,
(3) and a voltage controlled switch that selects one of two resistors.

An oscillating current source was not used because there appears to be no way to start or stop an ASPEC current source as a function of some condition (anode or gate voltage) other than an external time source. A FET model with a time varying transconductance that is a function of the internal TELD parameters and any external load would seem to be the optimum approach (see Recommendations). This approach was not used because to make transconductance time varying as a function of TELD internal parameters would require extensive internal modification of the ASPEC program which was not feasible within the time constraints and limited software access of this study. A voltage controlled switch proved to be an acceptable approach since the high field mobility of electrons in the TELD is less than the low field mobility resulting in an increased resistance under high field conditions.

Because the voltage controlled switch is the key element to this simulation, a short description is now presented. Figure 10 is a schematic of the switch. If the voltage across the controlling nodes, k1 and k2, is less

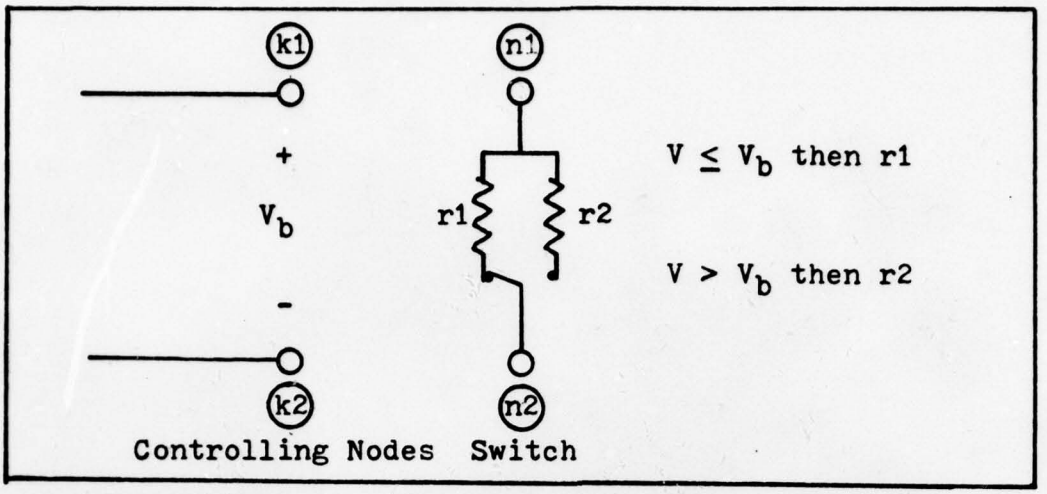


Figure 10. ASPEC voltage controlled switch (Ref 7:B-4).

than or equal to the break voltage V_b (an arbitrary value selected by the user) the switch is set to resistance r1, otherwise r2 is selected.

Figure 11 presents a generalized model of a TELD using a voltage controlled switch. When the device is properly biased, the voltage source begins to oscillate, causing the switch to alternate between r1 and r2. The magnitude of the current through the switch will depend on r1 and R_i while the frequency of operation will depend on the voltage source.

Circuit Model. Figure 12 is the circuit model that was devised to duplicate two terminal TELD operation. The TELD oscillator stages A, B, and C are shown in (a) and the TELD internal resistance circuit is shown in (b). Figure 13 presents the voltages at nodes 1, 3, and 4 as a function of time. All switches are positioned as shown for $t < 0$. All component values that are shown as variables may be adjusted

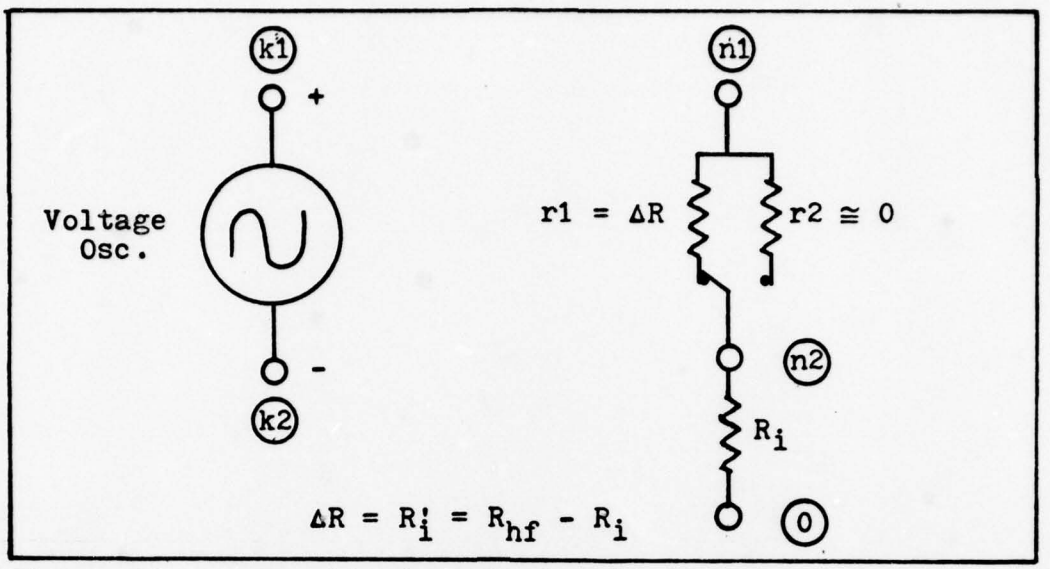


Figure 11. Generalized TELD circuit model.

to simulate a specific TELD. Actual equations for application of this model will be presented later. A value of 1 Giga Giga Ω is used to represent an open circuit. Any attempt to use 0 Ω caused computation problems in ASPEC.

Domain Formation Time. At $t < 0$ all capacitors are charged to their respective battery voltages and held there by the S#LL switches. When $t = 0$ the anode voltage (V_a is at node 12 and V'_a is used to isolate the oscillator from the TELD circuit) is sufficient to cause domain formation (V_{th} is exceeded) and switch SOVTH opens. C_o begins to discharge through R_{dco} to ground. When the voltage at node 1 is less than or equal to the break voltage (V_{b1}) for S1, S1 closes and C_1 discharges through R_{dc1} and R'_{dc1} until the voltage at node 4 is less than or equal to the break voltage for S1D. S1D switches to 1 Ω and C_1 discharges through R_{dc1}. R'_{dc1} introduces a time delay to allow C_o to

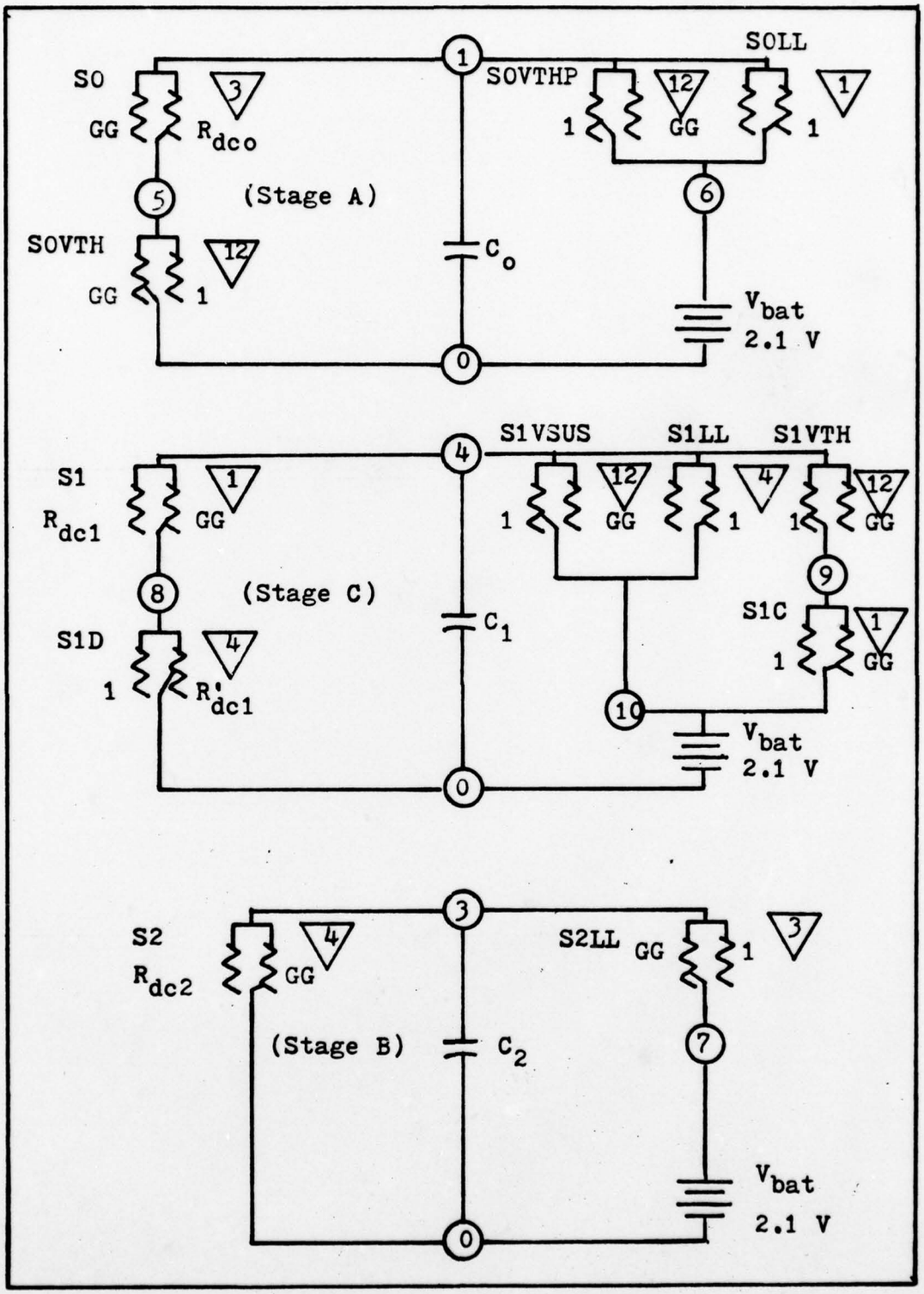
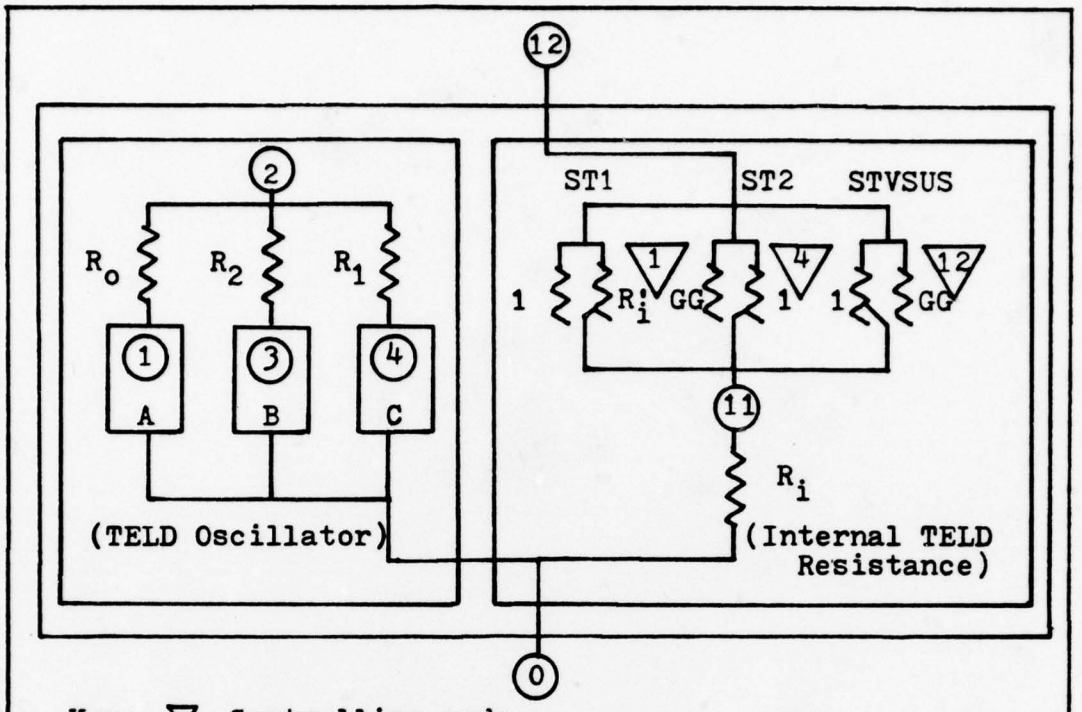


Figure 12a. Three stage TELD oscillator in sequence of control; A to C, C to B, B to A, etc.



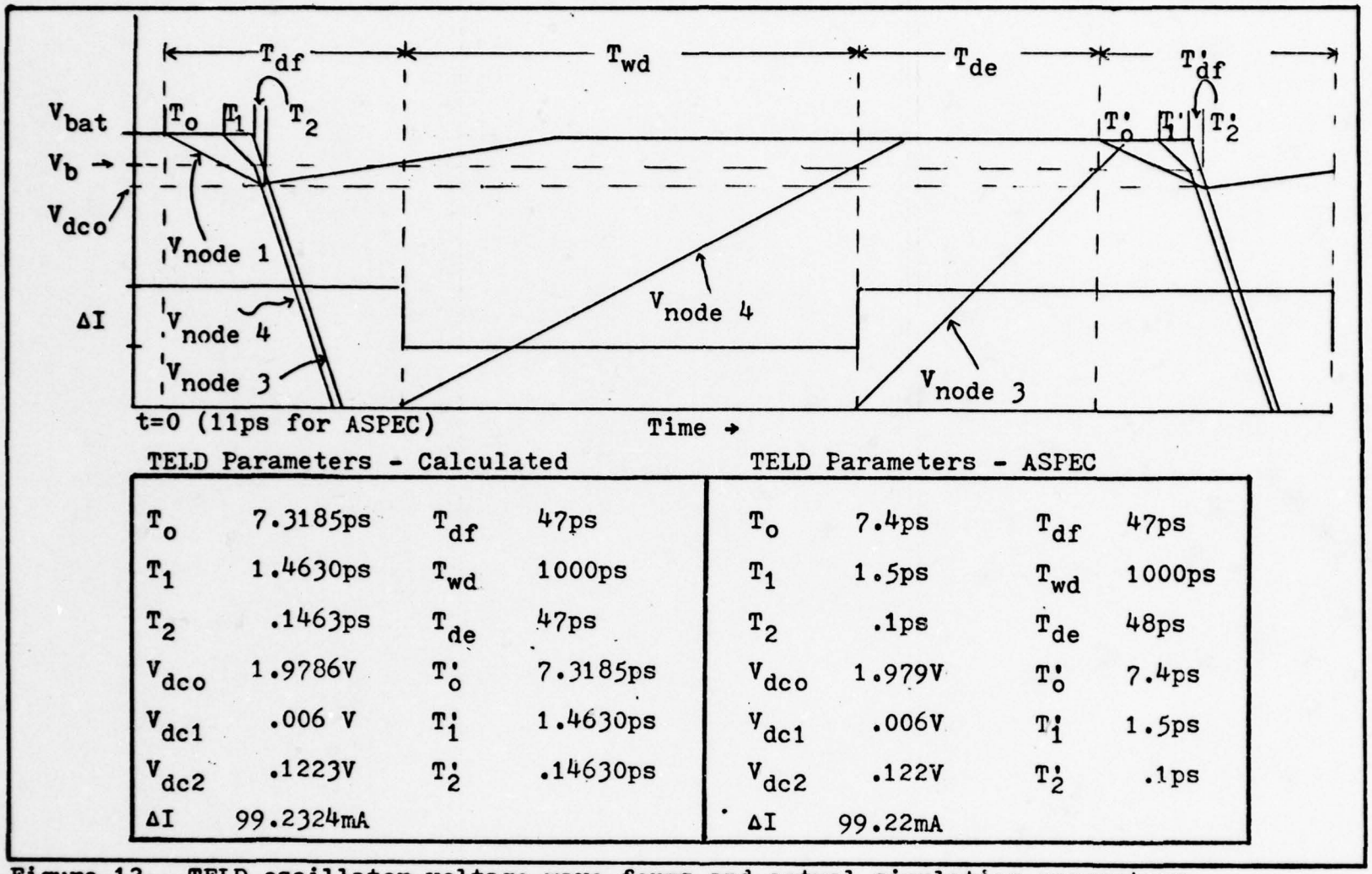
Key: ▽ Controlling node
GG Giga, Giga Ω - Defined as an open circuit

Switch	V_b	Switch	V_b
S0	2 V	S1D	2.00 V
S1	2 V	S2LL	2.10 V
S2	2 V	SOVTH	46.74 V
S1C	1.99 V	SOVTHP	46.74 V
S1LL	2.10 V	S1VTH	46.74 V
SOLL	2.10 V	S1VSUS	45.99 V

Figure 12b. Two terminal TELD shown as a macro containing a TELD oscillator and TELD internal resistances.

Table III.

R_{dco}	4999 Ω	R_o	2659.33 kΩ
R_{dc1}	99 Ω	R_1	764.62 kΩ
R'_{dc1}	901 Ω	R_2	38.11 kΩ
R_{dc2}	100 Ω	C_1	.03 pF
C_o	.03 pF	C_2	.03 pF



TELD Parameters - Calculated				TELD Parameters - ASPEC			
T_o	7.3185ps	T_{df}	47ps	T_o	7.4ps	T_{df}	47ps
T_1	1.4630ps	T_{wd}	1000ps	T_1	1.5ps	T_{wd}	1000ps
T_2	.1463ps	T_{de}	47ps	T_2	.1ps	T_{de}	48ps
V_{dco}	1.9786V	T'_o	7.3185ps	V_{dco}	1.979V	T'_o	7.4ps
V_{dc1}	.006 V	T'_1	1.4630ps	V_{dc1}	.006V	T'_1	1.5ps
V_{dc2}	.1223V	T'_2	.14630ps	V_{dc2}	.122V	T'_2	.1ps
ΔI	99.2324mA			ΔI	99.22mA		

Figure 13. TELD oscillator voltage wave forms and actual simulation parameters.

discharge to a value sufficiently small for proper operation. As the voltage at node 4 drops to, and below, V_{b2}, S2 switches to R_{dc2} and node 3 begins to discharge through R_{dc2}. Node 3 voltage drops from V_{bat} towards ground and as it passes through V_{bo}, SO switches open. C_o begins to charge through R_o. The voltage at node 1 rises to V_b for SOLL and it closes. The battery acts as a zener diode to maintain node 1 at V_{bat} after the node voltage passes V_{b1} and V_{bst1}. The time required for node 1 to decay and then charge to V_{b1} is the domain formation time T_{df}. See Figure 13.

At $t = 0$ ST1 of the TELD (see figure 12b) is set at R_i' until the voltage at node 1 is less than or equal to the break voltage for ST1, V_{bst1}. ST2 maintains the total internal resistance at R_i until the voltage at node 4 drops to V_{bst2} when ST2 opens and the total internal resistance becomes $R_i' + R_i$. Domain formation time is then complete.

The domain formation time of the circuit model is governed by the decay (T_{dco}) and rise (T_{rco}) times of the voltage at node 1. T_{dco} consists of the decay time of the voltage at node 1 from V_{bat} to V_{b1} (T_o), the decay time of the voltage at node 4 from V_{bat} to V_{b2} (T_1), and the decay time of the voltage at node 3 (T_2) from V_{bat} to V_{bo} where:

$$T_{dco} = T_o + T_1 + T_2 \qquad (17)$$

and

$$T_o = R_{dco}C_o \ln[(V_{bat}/V_{b1})] \quad (18)$$

$$T_1 = (R_{dc1} + R'_{dc1})C_1 \ln[(V_{bat}/V_{b2})] \quad (19)$$

$$T_2 = R_{dc2}C_2 \ln[(V_{bat}/V_{bo})]. \quad (20)$$

T_{rco} is the time required for node 1 to rise from V_{dco} to V_{b1}. Therefore,

$$T_{rco} = R_o C_o \ln[(V_a - V_{b1})/(V_a - V_{dco})] \quad (21)$$

where

$$V_{dco} = V_{bat} \exp[-T_{dco}/(R_{dco}C_o)]. \quad (22)$$

Domain Propagation Time. The end of T_{df} is defined as the time when the voltage at node 1 reaches V_{bst1} (and V_{b1}). The domain propagation time T_{wd} is defined as the rise time of the voltage at node 4 from V_{dc1} to V_{b2}. It is assumed that $R_{dc1}C_o$ is sufficiently small and T_{rco} is sufficiently long to allow the voltage at node 4 to decay to its lowest possible level, V_{dc1}. Note that T_{wd} is not total propagation time of the actual domain which begins as the domain forms and ends when the domain is completely extinguished. The domain propagation time T_{wd} is

$$T_{wd} = -R_1C_1 \ln[(V_a - V_{b2})/(V_a - V_{dc1})] \quad (23)$$

where

$$V_{dc1} = V_a[R_{dc1}/(R_1 + R_{dc1})]. \quad (24)$$

If the TELD channel length is very short such that T_{wd} is

approximately equal to T_{df} and T_{de} then,

$$V_{dc1} = V_{b2} \exp[-(T_{df} - (T_1 + T_o))/R_{dc1}C_1]. \quad (25)$$

Domain Extinction Time. Domain extinction time T_{de} is defined as beginning when the voltage at node 4 reaches V_{b2} and ending when the voltage at node 3 reaches V_{bo}. Domain extinction time is

$$T_{de} = R_2C_2\ln[(V_a - V_{bo})/(V_a - V_{dc2})] \quad (26)$$

where

$$V_{dc2} = V_a[R_{dc2}/(R_2 + R_{dc2})]. \quad (27)$$

If T_{df} and T_{wd} are so short as to not allow the voltage at node 3 to drop to its lowest possible level, then

$$V_{dc2} = V_{b2} \exp[-(T_{rco} + T_{wd})/R_{dc2}C_2]. \quad (28)$$

Operating Conditions. As stated previously, several conditions must be met to insure proper TELD operation. First, the triggering pulse must be at least equal to the domain formation time and have a magnitude equal to V_{th}. This condition is met by the S0VTH, S0VTHP, S1VTH, and the S1C switches. The TELD oscillator cannot begin to operate until the voltage at node 12 reaches V_{th} thereby closing S0VTH. Should the anode voltage (node 12) drop below V_{th} during T_{df}, S0VTHP, S1VTH, and S1C return their respective nodes to V_{bat} and the total TELD resistance is maintained at R_i. Any partial domain that may have formed during this

time must be extinguished before another is allowed to form (even if V_a goes above V_{th}) as SO will not close until the voltage at node 3 is above V_{bo}. This also prevents any new domain from forming before the previous one is extinguished during normal operation. Second, once the domain is triggered the anode voltage may drop below V_{th} but not V_{sus} to insure proper operation. Should the anode voltage drop below V_{th} but remain above V_{sus} after domain formation, SOVTH will open but have no effect on the circuit as SO is also open. Third, if the anode voltage then drops below V_{sus}, switch S1VSUS closes ending propagation and returning the internal TELD resistance to R_i, the low field resistance. Again, no new domain may form until the previous one is extinguished.

Actual Simulation of A Two Terminal TELD. The data in Table II were used to evaluate the circuit model in Figure 12. All capacitances were taken to be equal to C_d, the domain capacitance, and resistances were determined by equations (17) through (28). Values of R_{dco}, R_{dc1}, R'_{dc1}, and R_{dc2} had to be chosen to meet the following conditions (see Figure 13):

(1) C_o must decay from V_{bat} to less than V_{b1} in less than T_{df}.
(2) C_o must return to V_{bat} before the end of T_{de}.
(3) C_1 must rise to V_{bat} (after its inital decay to V_{dc1}) before the end of T'_o.
(4) C_2 must rise to V_{bat} before the end of T'_1.

Failure to meet the above conditions will result in the first cycle being longer than any subsequent cycles. A wide range of values for R_{dco}, R_{dc1}, R'_{dc1}, and R_{dc2} may be used. Table III shows the arbitrary values used for simulation.

Reducing equations (23) and (24) to solve for R_1 and equations (26) and (27) for R_2 produces two equations that are recursive in nature as R_1 and R_2 appear on both sides of their respective equations. The general form is

$$R_{\#} = T/C_{\#}\ln[(V_a - V_b)/(V_a - (V_a R_{dc\#}/(R_{dc\#} + R_{\#})))]. \quad (29)$$

A short program was developed that successively reduced the difference between a guess for $V_{dc\#}$ and $V'_{dc\#}$ calculated using equations (24) and (27) until ΔV_{dc} ($\Delta V_{dc} = V_{dc} - V'_{dc}$) was approximately zero. Figure 14 depicts the algorithm used. The program was developed and run on a TI Programmable 59 Calculator and is given in the Appendix. No run took more than twelve iterations to obtain a value of less than 10^{-6} for ΔV_{dc}.

Table III presents values for all the variables in the circuit model of Figure 12. Figure 15 shows the data as it was entered into ASPEC and Figure 16 is a composite of the data obtained during the computer simulation. Total CPU time (DEC 10 Computer) was approximately 1 minute 8 seconds for the transient response requested (see Figure 15 ".TRAN 10PS/10PS...."). Note that the TELD was declared as a macro with ports 0, 1, 3, 4, and 12. Ports 1, 3, and 4 were necessary to output the voltages at nodes 1, 3, and 4 while

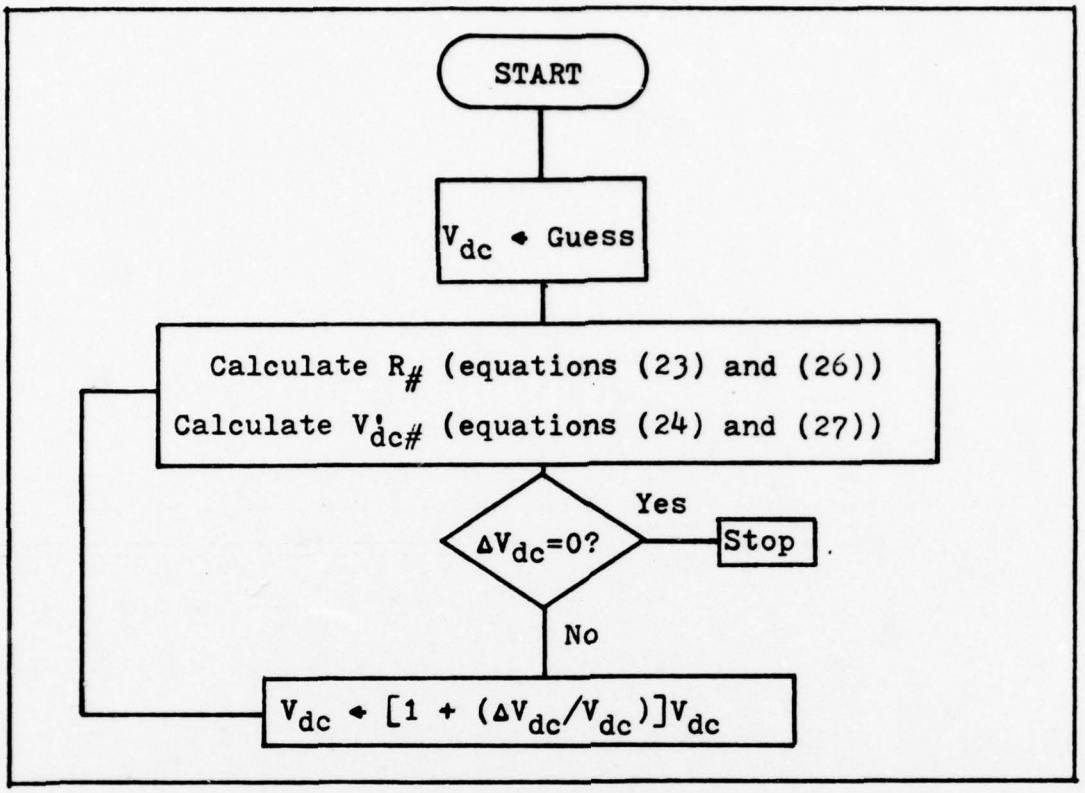


Figure 14. Algorithm for determining R_1 and R_2.

0 and 12 were necessary to apply the anode voltage.

The current through the TELD is represented by the symbol 3 in Figure 16 and is scaled as indicated. The anode voltage reaches threshold at 11 ps and is maintained. It is not necessary to maintain the anode at threshold after domain formation. The circuit model responds as predicted to threshold pulses of less than and greater than T_{df}. The model also reacts properly to anode voltages less than, equal to, or greater than V_{sus}.

Three Terminal TELD

The simulation of a three terminal TELD (addition of a gate) was very straightforward. One approach was to add

```
RICHARD ROACH   Two terminal TELD
.TRAN 10PS/10PS 1PS/30PS 10PS/50PS 1PS/60PS 10PS/1050PS
+ 1PS/1060PS 10PS/1100PS 1PS/1120PS 10PS/1150PS 1PS/1160

.PC BRIEF NP
.OP TRAN VOL
.CONTROL RMAX=.05
.OUTPUT 0 3 VC0 1 0 VC1 4 0 VC2 3 0 I*10 VANODE
.MACRO TELD   0 1 3 4 12
VANODEP    2     0 DC 0 PL 0/0 0/1PS 46.75/2PS
R0         2     1    2659.33K
C0         1     0    .03PF
S0         1     5    3    0       2V   NC 1GG      4999
SOLL       1     6    1    0    2.10V   NC 1GG       1
SOVTH      5     0    12   0   46.74V   NO 1GG       1
SOVTHP     1     6    12   0   46.74V   NC 1         1GG
B0         6     0    2.10V .1
R2         2     3    38.11K
C2         3     0    .03PF
S2         3     0    4    0       2V   NO 100       1GG
S2LL       3     7    3    0     2.1V   NC 1GG       1
B2         7     0    2.10V .1
R1         2     4    764.62K
C1         4     0    .03PF
S1         4     8    1    0       2V   NO 99        1GG
S1D        8     0    4    0       2V   NC 1         901
S1LL       4    10    4    0     2.1V   NC 1GG       1
S1VSUS     4    10   12    0   46.74V   NC 1         1GG
S1VTH      4     9   12    0   46.74V   NC 1         1GG
S1C        9    10    1    0    1.99V   NO 1         1GG
B1        10     0   2.10V .1
ST1       12    11   1     0       2V   NO .1        560
ST2       12    11   4     0       2V   NC 1GG       .1
STVSUS    12    11   12    0   46.74V   NO 1         1GG
RI        11     0   305
.EOM
XTELD 0 1 3 4 12 TELD
VANODE   12 0 DC 0 PL 0/0 0/1PS 46/2PS 46/10.99PS 46.75/11
.END
```

Figure 15. Two Terminal TELD data as entered into ASPEC.

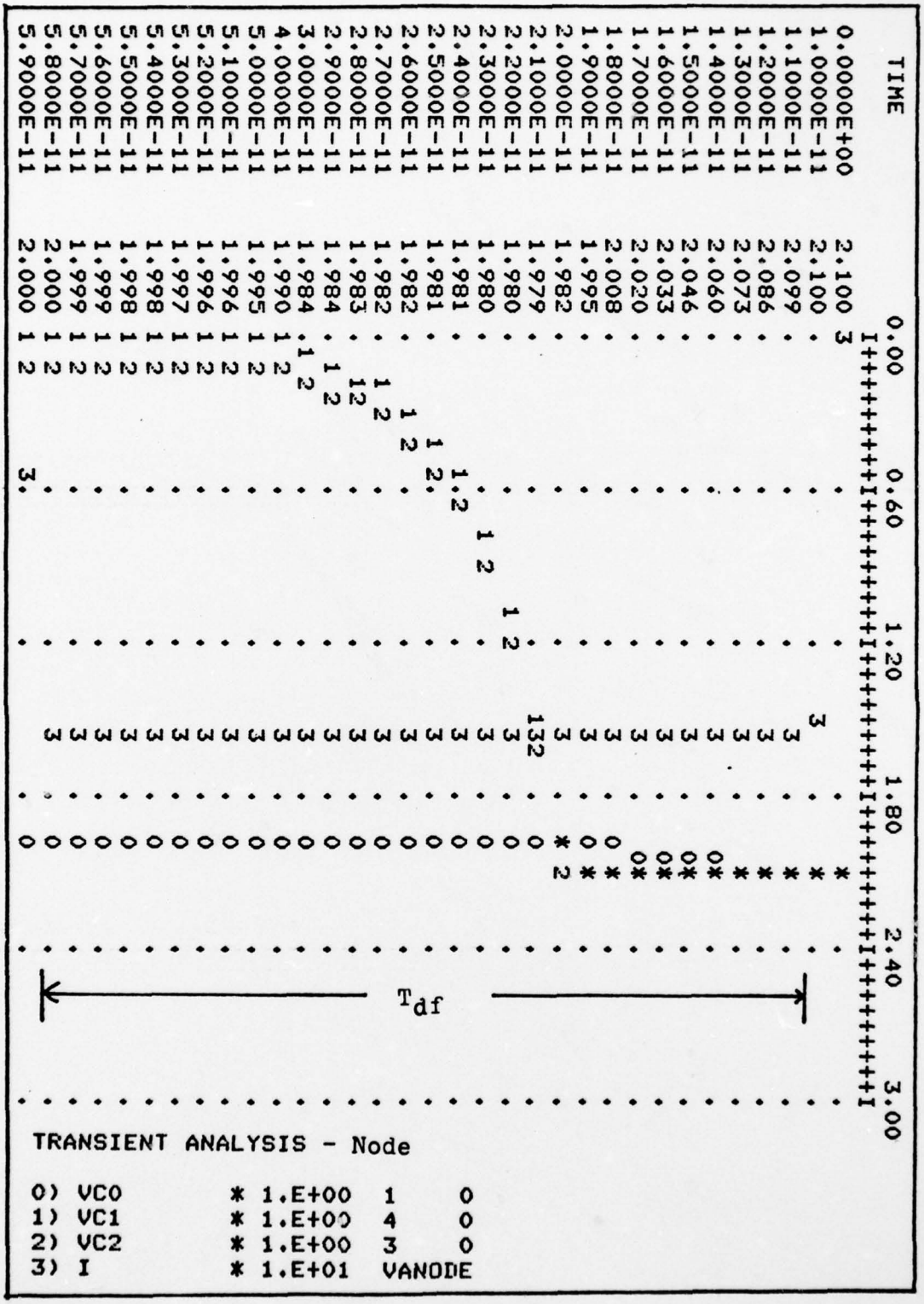
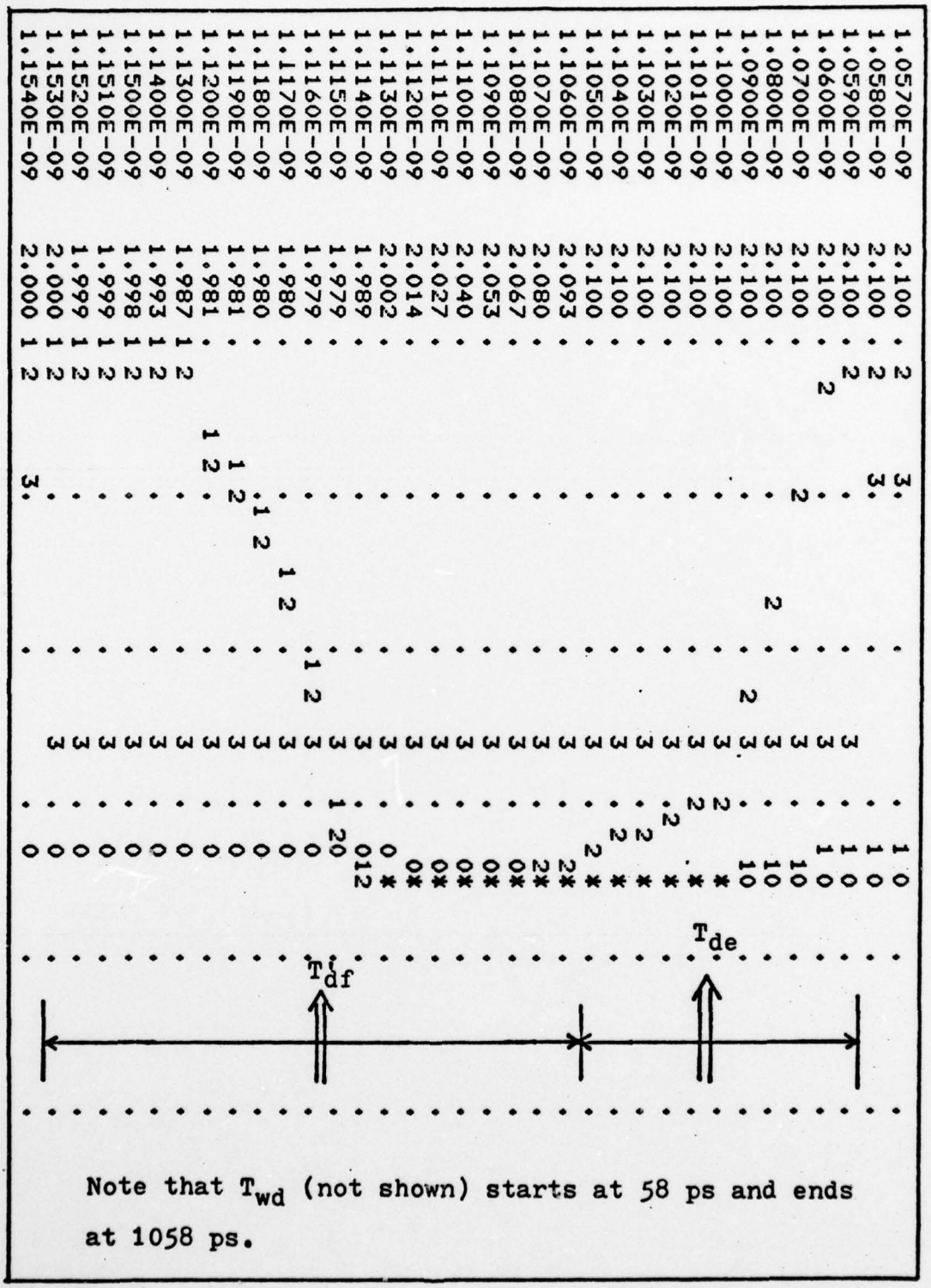


Figure 16. Node voltages versus time.



Note that T_{wd} (not shown) starts at 58 ps and ends at 1058 ps.

Figure 16. Continued.

gate voltage controlled switches (S#VG) in combination with the threshold switches (S#VTH) to maintain proper operation under control of the gate and anode voltages. The approach taken was to assume that the anode voltage would not be used for logic operation and all logic functions would be controlled by the gate. The S#VTH switches were renamed "S#VG" and their break voltages set at V_g (see Table I).

Figure 17 is the data entered into ASPEC for the gate controlled TELD. In the computer simulation the gate voltage was applied at 11 ps as in the simulation for the two terminal TELD. As the active channel in the three terminal TELD was the same as that for the two terminal (85 μm), the operational parameters remained the same and Figure 16 is a duplicate of the data obtained for the three terminal device. It should be noted that additional channel resistance due to depletion under the gate prior to domain formation was not replicated for simplicity. This accounts for the apparent discrepancy between simulation results and threshold (I_{tho}) and output (I_{og}) currents of Table I. For simulation it is assumed that no depletion of the channel occurs until a gate voltage is applied.

Simulation of Three Terminal TELD AND Gate. Figure 18a depicts a dual gated, three terminal TELD configuration that can be used as either an AND or an OR gate. Figure 18b shows the AND or OR configuration as it is used as a macro for simulation using ASPEC. Resistors R_{g1} and R_{g2} are load resistors for gate supply voltages V_{g1} and V_{g2}. R_{g1} and R_{g2}

```
.PC BRIEF NP
.OP TRAN VOL
.CONTROL RMAX=.02
.OUTPUT 0 3 VC0 1 0 VC1 4 0 VC2 3 0 I*10 VANODE
.MACRO TELD  0 1 3 4 12 13
VANODEP    2     0 DC 0 PL 0/0 0/1PS 46.75/2PS
R0         2     1    2659.33K
C0         1     0    .03PF
S0         1     5    3    0       2V   NC 1GG       4999
SOLL       1     6    1    0    2.10V   NC 1GG       1
SOVG       5     0    13   0   -3.99V   NO 1         1GG
SOVGP      1     6    13   0   -3.99V   NC 1GG       1
B0         6     0    2.10V .1
R2         2     3    38.11K
C2         3     0    .03PF
S2         3     0    4    0       2V   NO 100       1GG
S2LL       3     7    3    0     2.1V   NC 1GG       1
B2         7     0    2.10V .1
R1         2     4    764.62K
C1         4     0    .03PF
S1         4     8    1    0       2V   NO 99        1GG
S1D        8     0    4    0       2V   NC 1         901
S1LL       4    10    4    0     2.1V   NC 1GG       1
S1VSUS     4    10   12    0   46.00V   NC 1         1GG
S1VG       4     9   13    0   -3.99V   NC 1GG       1
S1C        9    10    1    0    1.99V   NO 1         1GG
B1        10     0   2.10V .1
ST1       12    11   1     0       2V   NO .1        560
ST2       12    11   4     0       2V   NC 1GG       .1
STVSUS    12    11   12    0   46.00V   NO 1         1GG
RI        11     0   305
RX        13     0   1G
.EOM
XTELD 0 1 3 4 12 13 TELD
VANODE   12 0 DC 0 PL 0/0 0/1PS 46.75/2PS
VGATE    13 0 DC 0 PL 0/0 0/10PS -4/10.99PS
.END
```

Figure 17. Gated controlled TELD.

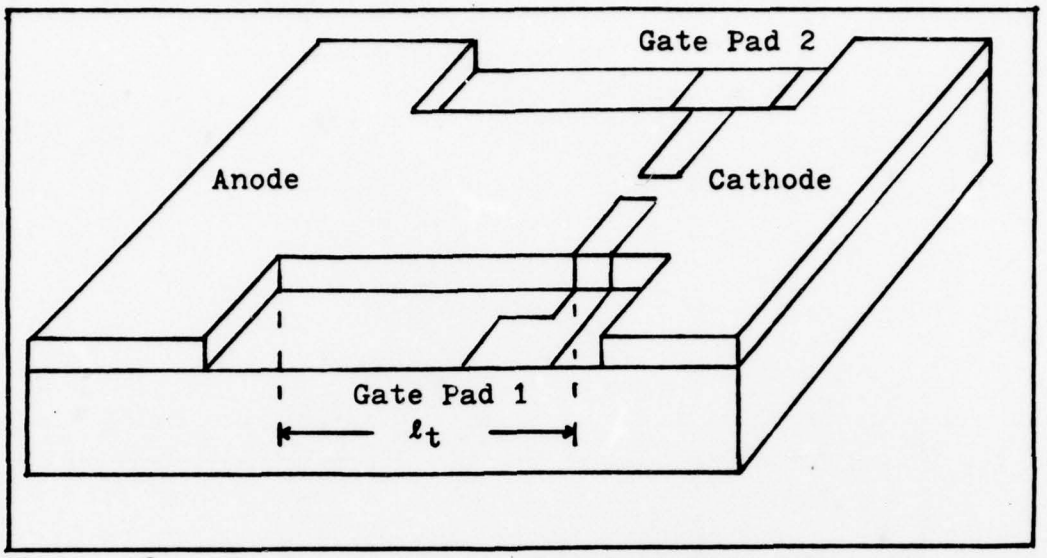


Figure 18a. Dual gated three terminal TELD AND or OR gate.

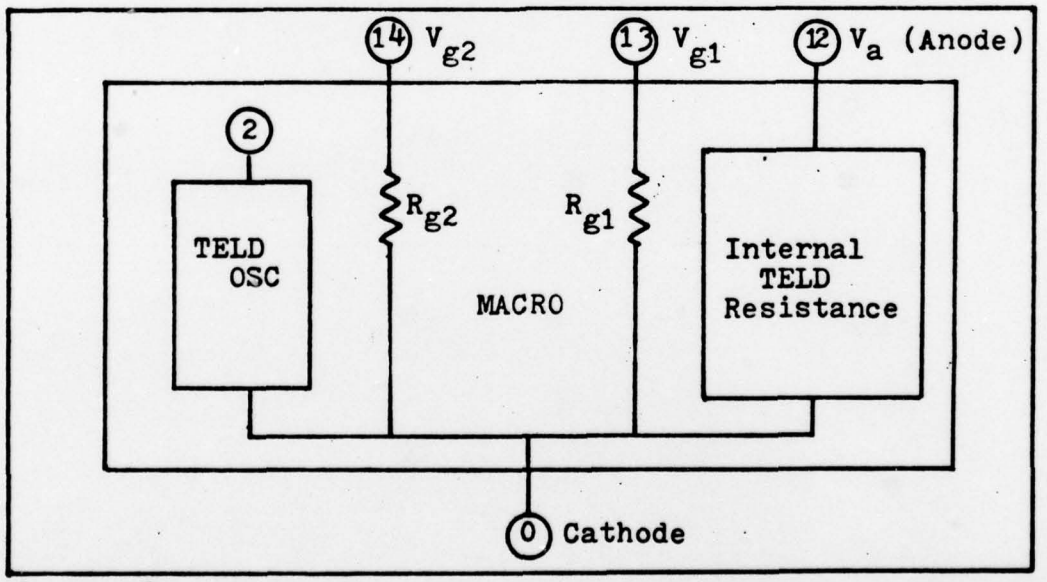


Figure 18b. Macro for a three terminal TELD AND or OR gate.

prevent error messages when using ASPEC and have no effect on the operation of the circuit. Data in Table I is the basis for simulation.

In AND gate operation, sufficient depletion of the active channel for domain formation requires that both gates be on (assumed to less than -3.99 V for both gates for simulation) (Ref 5:927). Figure 19 shows the required changes in the TELD oscillator stages. In stage A, C_o cannot discharge (simulating domain charging) unless both S0VG1 (controlled by V_{g1}, node 13) and S0VG2 (controlled by V_{g2}, node 4) are caused to switch closed by their respective gate voltages, thus simulating depletion of the channel under the gates. Switches S0VG1P and S0VG2P maintain node 1 at V_{bat} until both gates are sufficient to cause domain formation. In stage C, S1VG1 and S1VG2 are added to simulate cessation of domain propagation if either gate voltage switches to the off state (greater than or equal to -3.99 V for simulation) during domain formation. The internal resistance is maintained at R_i. The S1VG# switches act in concert with the S1C switch just as the S1VTH switch does for the two terminal TELD as previously described. No additional switches were required for stage B of the oscillator or the internal TELD resistance circuit. Figure 20 is the three terminal TELD AND gate data as it is entered into ASPEC.

The only constraint discovered by simulation of AND operation is that the last gate to turn on (V_{g2}, Figure 21) determines when domain formation begins so the first gate to

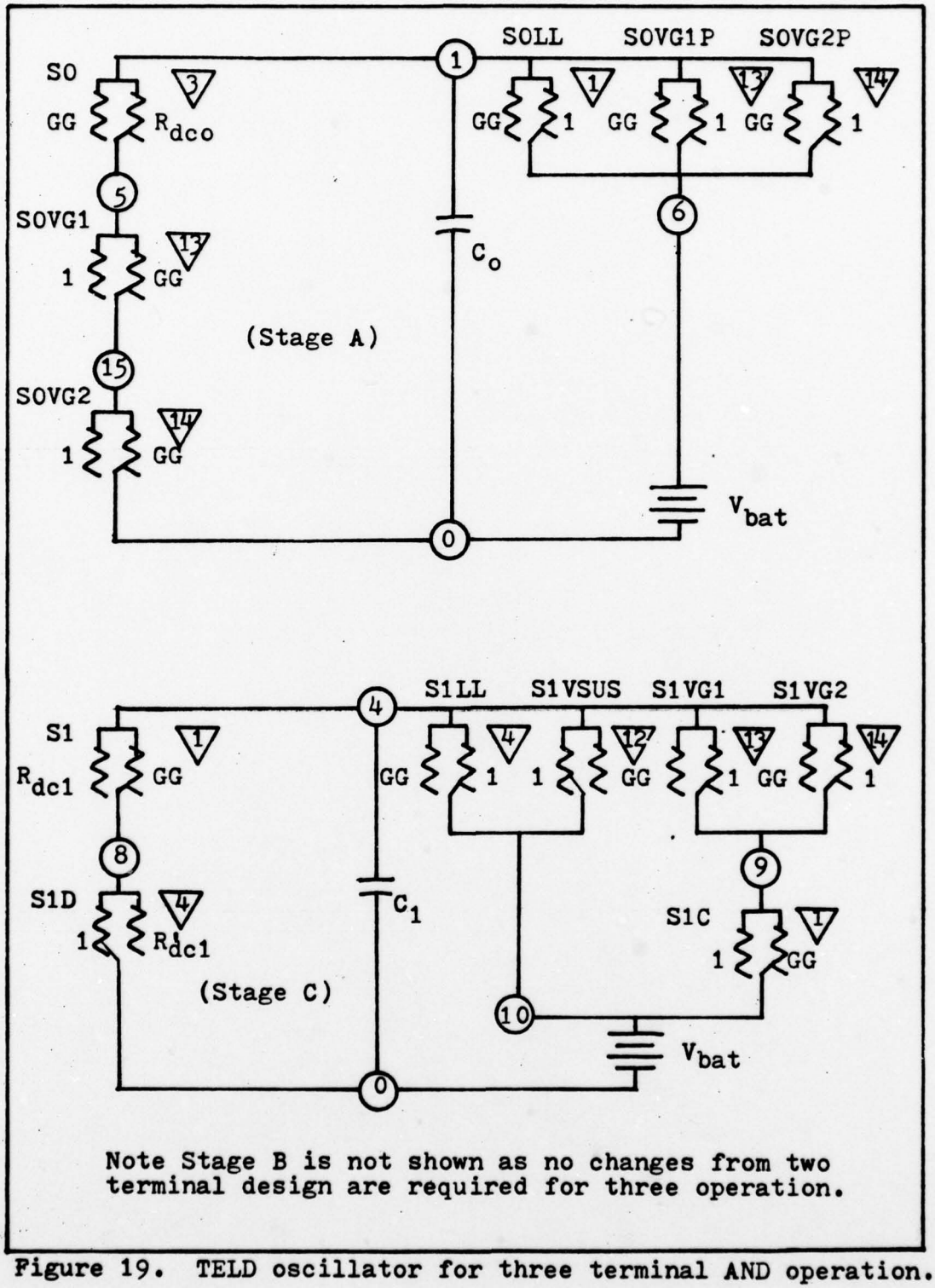


Figure 19. TELD oscillator for three terminal AND operation.

```
THREE TERMINAL TELD AND GATE
.TRAN 5PS/200PS

.PC BRIEF NP
.OP TRAN VOL
.CONTROL RMAX=.05
.OUTPUT -2.5 2.5 I*10 VANODE
+ V1*.25 13 0 V2*.25 14 0
.MACRO TELD  0 1 3 4 12 13 14
VANODEP    2     0 DC 0 PL 0/0 0/1PS 46.75/2PS
RO         2     1    2659.33K
CO         1     0    .03PF
SO         1     5    3    0       2V   NC 1GG       4999
SOLL       1     6    1    0    2.10V   NC 1GG       1
SOVG1      5    15   13    0   -3.99V   NO 1         1GG
SOVG2     15     0   14    0   -3.99V   NO 1         1GG
SOVGP1     1     6   13    0   -3.99V   NC 1GG       1
SOVGP2     1     6   14    0   -3.99V   NC 1GG       1
BO         6     0    2.10V .1
R2         2     3    38.11K
C2         3     0    .03PF
S2         3     0    4    0       2V   NO 100       1GG
S2LL       3     7    3    0     2.1V   NC 1GG       1
B2         7     0    2.10V .1
R1         2     4    764.62K
C1         4     0    .03PF
S1         4     8    1    0       2V   NO 99        1GG
S1D        8     0    4    0       2V   NC 1         901
S1LL       4    10    4    0     2.1V   NC 1GG       1
S1VSUS     4    10   12    0   46.00V   NC 1         1GG
S1VG1      4     9   13    0   -3.99V   NC 1GG       1
S1VG2      4     9   14    0   -3.99V   NC 1GG       1
S1C        9    10    1    0    1.99V   NO 1         1GG
B1        10     0    2.10V .1
ST1       12    11    1    0       2V   NO .1        560
ST2       12    11    4    0       2V   NC 1GG       .1
STVSUS    12    11   12    0   46.00V   NO 1         1GG
RI        11     0    305
RX        13     0    1G
RX1       14     0    1G
.EOM
XTELD 0 1 3 4 12 13 14 TELD
VANODE   12 0 DC 0 PL 0/0 0/1PS 46.75/2PS
VGATE1   13 0 DC 0 PL 0/0 0/10PS -4/10.01PS
VGATE2   14 0 DC 0 PL 0/0 0/70PS -4/70.01PS
.END
```

Figure 20. Three terminal TELD AND gate data for ASPEC.

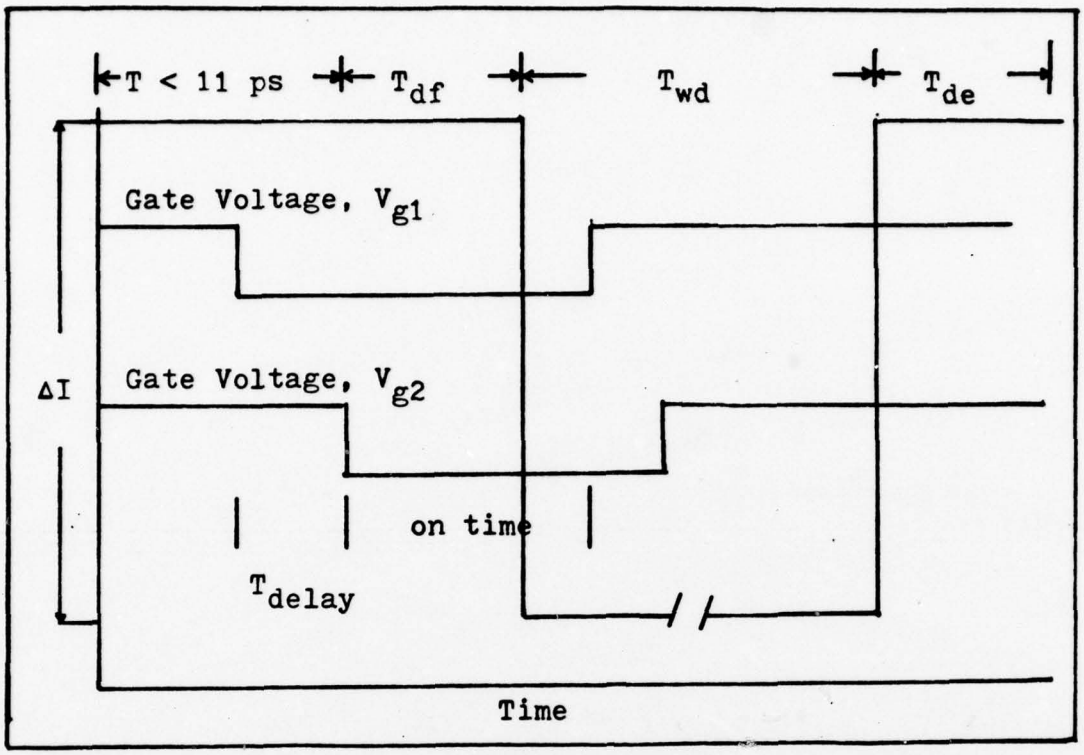


Figure 21. Three terminal TELD AND gate timing chart.

reach the on state (V_{g1}, Figure 21) must remain on for a period of time to include any time delay T_{delay} between the two gates and the domain formation time. Both gates must be on for a period of time greater than the domain formation time of the device being triggered. The timing constraint between gates discovered by simulation should apply to actual devices although there seems to be no discussion of it presented in literature on three terminal TELD AND operation. Figure 21 is a composite of the timing diagram for AND operation as simulated by ASPEC. T_{df}, T_{wd}, T_{de} and ΔI remain the same as that for two terminal operation. V_{g2} starts domain formation at 11 ps, therefore, exact values of the domain propagation characteristics can be obtained from

Figure 16.

Simulation of Three Terminal TELD OR Gate. In OR gate operation sufficient depletion of the active channel for domain formation requires that only one gate be on. See Figure 18 for configuration and ASPEC macro declaration. Figure 22 shows the required changes in the TELD oscillator stages. In stage A if either S0VG1 or S0VG2 switches closed (simulating channel depletion), C_o is allowed to discharge simulating domain formation. S0VG1P and S0VG2P maintain node 1 at V_{bat} until either switch opens. In stage C the S1VG1 and S1VG2 switches are added in series with the S1C switch. Should a gate voltage switch from the on state to the off state before domain formation while the other gate remains off, the appropriate S1VG# switch and the S1C switch return node 4 to V_{bat} and the total internal TELD resistance is maintained at R_i. Should the on time of each gate overlap such that the total on time is greater than T_{df}, domain formation will proceed even though the first gate to turn on turns off prior to T_{df}. Figure 23 is the OR data as entered into ASPEC and Figure 24 is a composite timing diagram of OR TELD operation simulated by ASPEC. Figure 16 may be used to obtain exact data produced by ASPEC.

Four Terminal TELD

As was mentioned in the discussion on depletion operation, the voltage output of a TELD (obtained by series addition of a load resistor) is not compatible with gate voltage requirements of any follow-on TELD. The addition of

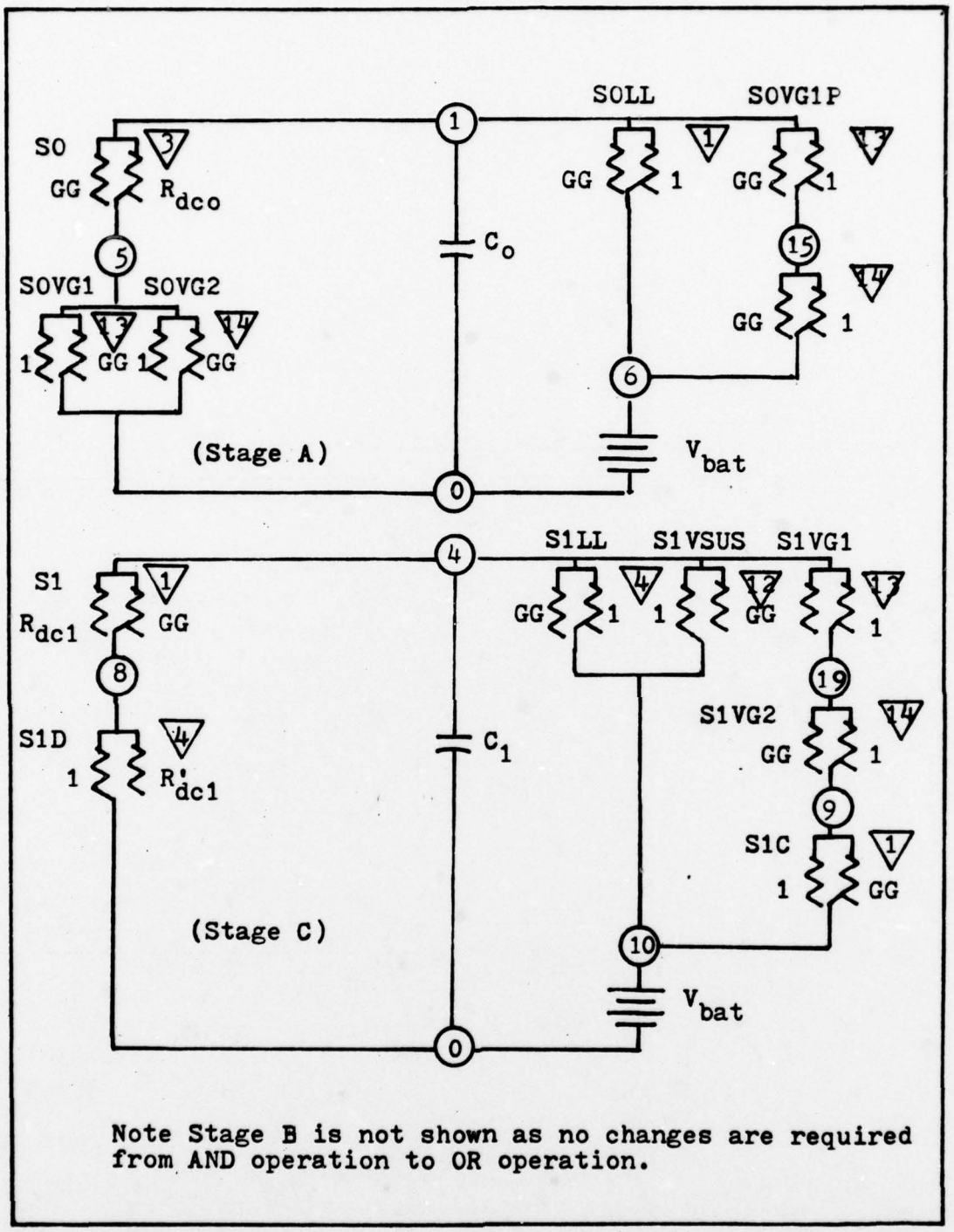


Figure 22. TELD oscillator for three terminal OR operation.

```
THREE TERMINAL TELD OR GATE
.TRAN 5PS/200PS

.PC BRIEF NP
.OP TRAN VOL
.CONTROL RMAX=.05
.OUTPUT -2.5 2.5 I*10 VANODE
+ V1*.25 13 0 V2*.25 14 0
.MACRO TELD  0 1 3 4 12 13 14
VANODEP    2     0 DC 0 PL 0/0 0/1PS 46.75/2PS
R0         2     1    2659.33K
C0         1     0    .03PF
S0         1     5    3    0       2V   NC 1GG        4999
SOLL       1     6    1    0    2.10V   NC 1GG        1
SOVG1      5     0    13   0   -3.99V   NO 1          1GG
SOVG2      5     0    14   0   -3.99V   NO 1          1GG
SOVGP1     1    15    13   0   -3.99V   NC 1GG        1
SOVGP2     15    6    14   0   -3.99V   NC 1GG        1
B0         6     0    2.10V .1
R2         2     3    38.11K
C2         3     0    .03PF
S2         3     0    4    0       2V   NO 100        1GG
S2LL       3     7    3    0     2.1V   NC 1GG        1
B2         7     0    2.10V .1
R1         2     4    764.62K
C1         4     0    .03PF
S1         4     8    1    0       2V   NO 99         1GG
S1D        8     0    4    0       2V   NC 1          901
S1LL       4    10    4    0     2.1V   NC 1GG        1
S1VSUS     4    10   12    0   46.00V   NC 1          1GG
S1VG1      4    19   13    0   -3.99V   NC 1GG        1
S1VG2      19    9   14    0   -3.99V   NC 1GG        1
S1C        9    10    1    0    1.99V   NO 1          1GG
B1         10    0   2.10V .1
ST1        12   11   1     0       2V   NO .1         560
ST2        12   11   4     0       2V   NC 1GG        .1
STVSUS     12   11   12    0   46.00V   NO 1          1GG
RI         11    0   305
RX         13    0   1G
RX1        14    0   1G
.EOM
XTELD 0 1 3 4 12 13 14 TELD
VANODE   12 0 DC 0 PL 0/0 0/1PS 46.75/2PS
VGATE1   13 0 DC 0 PL 0/0 0/10PS -4/10.01PS
VGATE2   14 0 DC 0 PL 0/0 0/90PS -4/90.01PS
.END
```

Figure 23. Three terminal TELD OR gate data for ASPEC

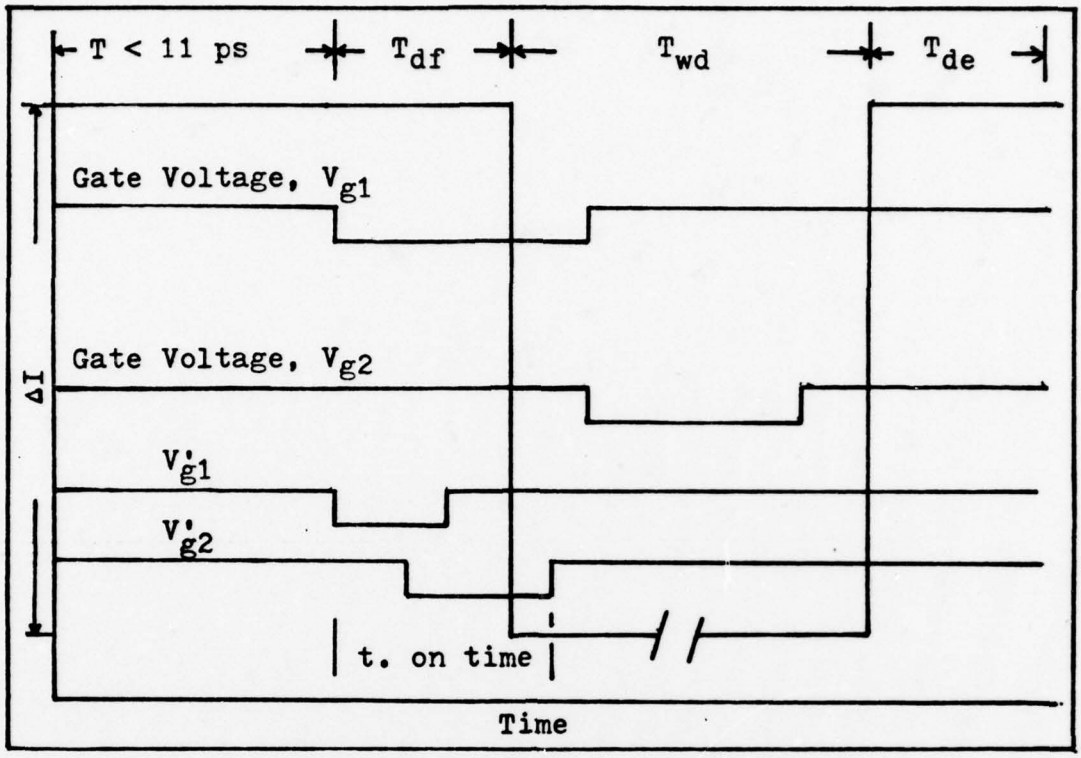


Figure 24. Three terminal TELD OR gate timing chart.

a capacitive electrode near the anode can be used to trigger another TELD because the potential under the electrode drops by the amount of the domain voltage as the domain passes under the contact. Figure 25 shows four terminal TELD configuration. The length of the electrode necessary to trigger other TELDs is determined by domain size, domain velocity, and the domain formation time of the follow-on TELD, T'_{df}. Because OR operation requires only one gate to trigger TELD operation, the four terminal TELD OR gate model was used to simulate basic four terminal operation and the discussion in this section will include OR operation.

Figure 26 shows domain shapes for various peak domain fields. If it is assumed that the potential drop of the

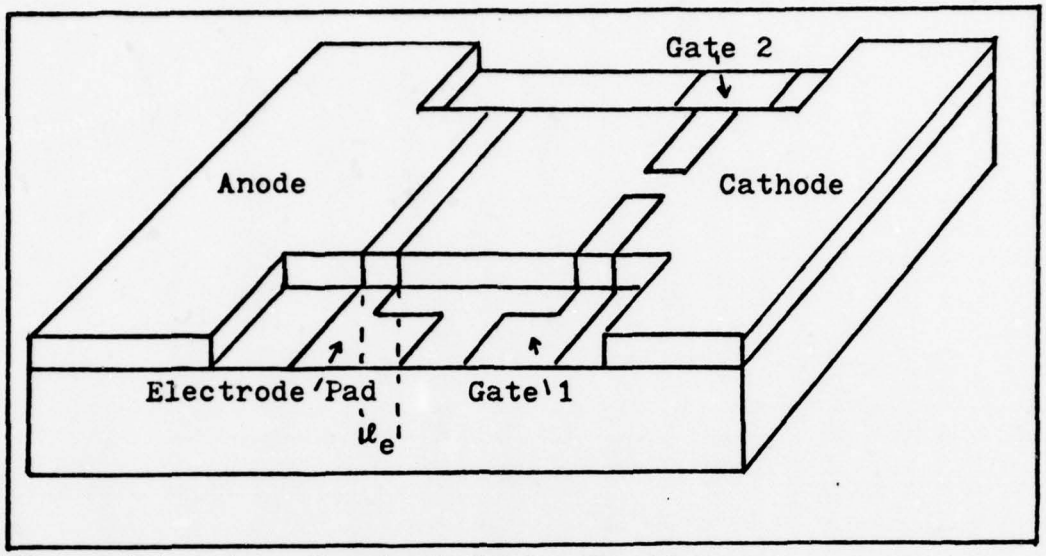


Figure 25. Four Terminal TELD AND, OR gate.

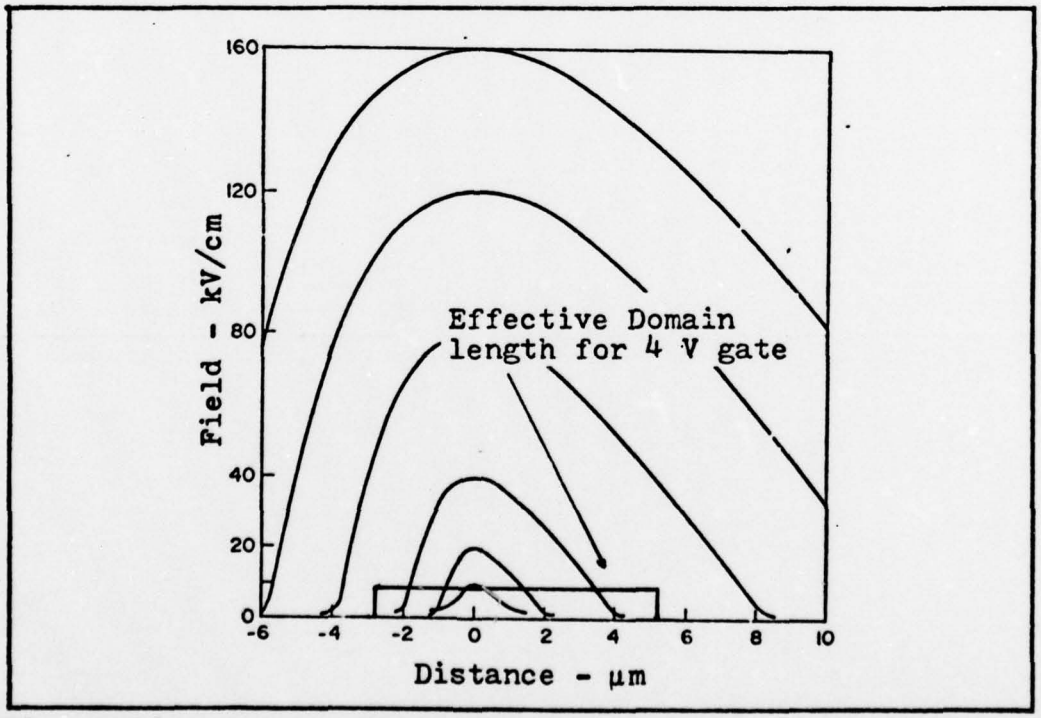


Figure 26. Domain shapes for various peak domain fields (Ref 8:122).

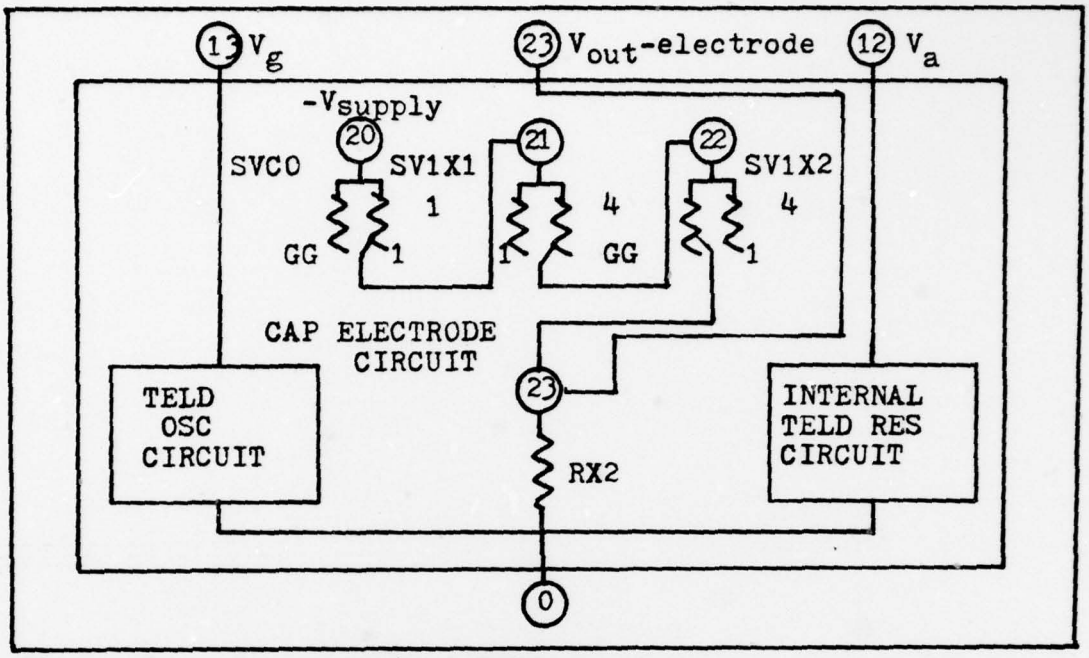


Figure 27. Four terminal TELD macro.

capacitive electrode is exactly equal to the domain potential when the domain passes under the electrode, the effective length of the domain can be estimated. From Figure 4 the estimated domain potential of the device described in Table I is 45 V and the gate voltage is -4 V. From Figure 25 the effective domain length is approximately 8 μm. The domain velocity for the TELD of Table I is 7.77×10^{10} μm/s (85 μm/1094 ps) and if identical TELDs are used, T'_{df} is 47 ps. If it is assumed that full gate voltage cannot be reached until the domain is completely under the electrode, an electrode length of 16 μm will produce about 103 ps of gate voltage, sufficient to trigger follow-on TELDs, as the domain travels 8 μm while completely under the electrode.

To simulate the operation of the capacitive electrode, an electrode circuit (see Figure 27) consisting of three

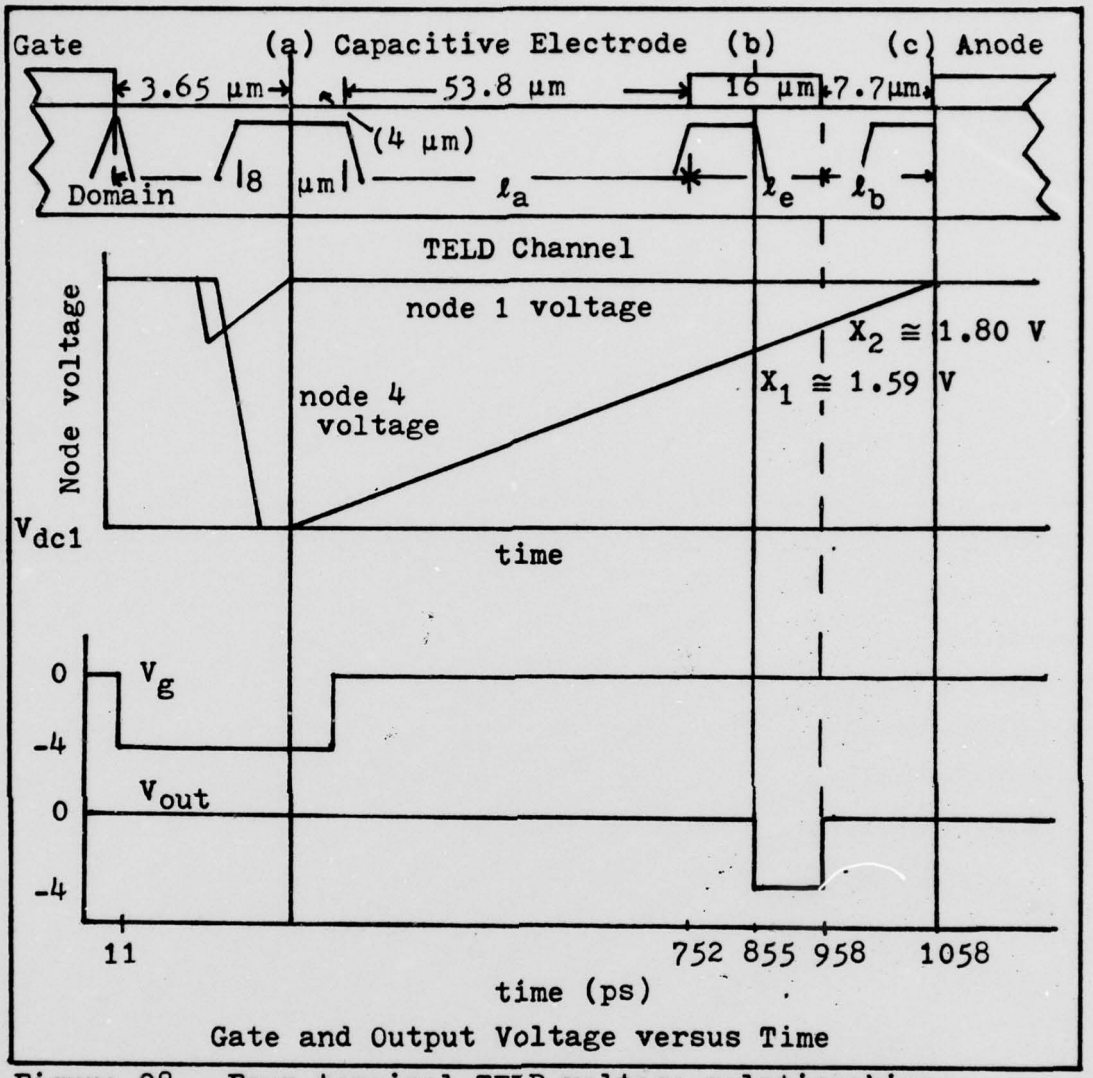


Figure 28. Four terminal TELD voltage relationships.

switches was added to the three terminal TELD macro. The rise of the voltage at node 4 of the oscillator shown in Figure 28 represents domain propagation time T_{wd}. Switch SV1X1 closes when the voltage at node 4 is greater than X_1. Switch SV1X2 closes when the node voltage is equal to or less than X_2. The time required for the voltage at node 4 to pass from X_1 through X_2 represents the effective time (capable of triggering another TELD) the domain is under the

capacitive electrode. During simulated domain formation, the voltage at node 4 drops through X_2 and X_1. Switch SVC0 is controlled by node 1 such that it is open when the voltage is less than or equal to 2 volts. The supply voltage ($-V_{supply}$) of the capacitive electrode circuit is simulated as passing under the output contact.

Size and placement of the electrode for simulation depends on the voltage values for X_1 and X_2 because distance is directly related to the time required for the domain to pass certain points on the active channel. Because the domain is expanding as it propagates during domain formation, it is approximately in position (a) of Figure 28 when formation is complete. The distance from the gate to the leading edge of the electrode in terms of the TELD model oscillator parameters is

$$\ell_a = [[-R_1C_1\ln(V_a - X_1)/(V_a - V_{dc1})] + T_{df}]V_{domain} - \ell_d/2 \qquad (29)$$

where V_{domain} is domain velocity, ℓ_d is domain length, and V_{dc1} is determined by either equation (24) or (25). At point (b) the domain is completely under the electrode and capable of providing sufficient gate voltage to a follow-on TELD (SV1X1 closes in the circuit model). The length of the capacitive electrode is, therefore,

$$\ell_e = [-R_1C_1\ln((V_a - X_2)/(V_a - X_1))]V_{domain} + \ell_d. \qquad (30)$$

When the leading edge of the domain contacts the anode, the

domain is in position (c). The distance from the trailing edge of the electrode to the leading edge of the anode is

$$\ell_b = -R_1 C_1 \ln[(V_a - V_{b2})/(V_a - X_2)]V_{domain} \qquad (31)$$

where V_{b2} is the break voltage for S2 of the oscillator and ST1 of the internal TELD resistance circuit which determines the end of T_{wd}. For simulation placement of the electrode was arbitrarily made as shown in Figure 28. Included in Figure 28 is a timing chart of four terminal TELD operation as simulated by ASPEC. Note V_{out} is shown as -4 V. K. Mause (Ref 5:927) states that the drop of potential under the electrode should be equal to domain potential, producing a corresponding drop of 45 V. For simulation -4 V was used as the minimum voltage necessary to trigger follow-on TELDs. Figure 29 is the data for a four terminal TELD (and OR gate) as entered into ASPEC.

OR operation of the four terminal TELD produced no unusual conditions besides those discussed under three terminal TELD operation. It is apparent from Figure 28 that four terminal operation in general will have signal pulse delays per stage of domain formation time and domain propagation time of the domain to a point under the capacitive electrode where sufficient voltage is produced to trigger domain formation in the next TELD.

Simulation of Four Terminal TELD AND Gate. AND operation for the four terminal TELD was accomplished by the addition of the capacitive electrode circuit previously

```
FOUR TERMINAL TELD OR GATE
.TRAN 10PS/900PS 5PS/1100PS

.PC BRIEF NP
.OP TRAN VOL
.CONTROL RMAX=.05
.OUTPUT -2.5 2.5 VC1 4 0 I*10 VANODE VOUT*.5 23 0
.MACRO TELD  0 1 3 4 12 13 14 23
VANODEP    2     0  DC 0 PL 0/0 0/1PS 46.75/2PS
R0         2     1    2659.33K
C0         1     0    .03PF
S0         1     5    3    0       2V   NC 1GG       4999
SOLL       1     6    1    0    2.10V   NC 1GG       1
SOVG1      5     0    13   0   -3.99V   NO 1         1GG
SOVG2      5     0    14   0   -3.99V   NO 1         1GG
SOVGP1     1    15    13   0   -3.99V   NC 1GG       1
SOVGP2    15     6    14   0   -3.99V   NC 1GG       1
B0         6     0    2.10V .1
R2         2     3    38.11K
C2         3     0    .03PF
S2         3     0    4    0       2V   NO 100       1GG
S2LL       3     7    3    0     2.1V   NC 1GG       1
B2         7     0    2.10V .1
R1         2     4    764.62K
C1         4     0    .03PF
S1         4     8    1    0       2V   NO 99        1GG
S1D        8     0    4    0       2V   NC 1         901
S1LL       4    10    4    0     2.1V   NC 1GG       1
S1VSUS     4    10   12    0   46.00V   NC 1         1GG
S1VG1      4    19   13    0   -3.99V   NC 1GG       1
S1VG2     19     9   14    0   -3.99V   NC 1GG       1
S1C        9    10    1    0    1.99V   NO 1         1GG
B1        10     0   2.10V .1
ST1       12    11    1    0       2V   NO .1        560
ST2       12    11    4    0       2V   NC 1GG       .1
STVSUS    12    11   12    0   46.00V   NO 1         1GG
RI        11     0   305
RX        13     0   1G
RX1       14     0   1G
RX2       23     0   10K
VGOUT     20     0   0 DC 0 PL 0/0 0/1PS -4.01/2PS
SVCO      20    21    1    0       2V   NC 1GG       1
SV1X2     21    22    4    0    1.98V   NO 1         1GG
SV1X1     22    23    4    0    1.78V   NO 1GG       13
.EOM
XTELD 0 1 3 4 12 13 14 23 TELD
VANODE   12 0 DC 0 PL 0/0 0/1PS 46.75/2PS
VGATE1   13 0 DC 0 PL 0/0 0/10PS -4/10.01PS
VGATE2   14 0 DC 0 PL 0/0 0/90PS -4/90.01PS
.END
```

Figure 29. Four Terminal OR Gate data for ASPEC.

described to the three terminal TELD AND gate. Simulation results were exactly the same as those obtained for three terminal operation with the exception of the time delay incurred while the domain propagates to the capacitive electrode. Three and four terminal AND simulation produced identical results for T_{df}, T_{wd}, T_{de}, and ΔI which were also identical to two terminal simulation results. Four terminal AND data may be obtained from Figures 16, 21, and 28. Figure 28 shows the time delay for V_{out}. Figure 30 presents the four terminal AND gate data as it was entered into ASPEC.

Simulation of A Dynamic Shift Register. Using four terminal TELD AND gates declared as macros, an attempt was made to simulate a dynamic shift register that was proposed and successfully monolithically integrated by K. Mause (Ref 5:926). Figure 31 depicts the shift register which consists of AND gates followed by a delay structure. Since the time delay per stage is T_{df} plus propagation time to the capacitive electrode, which is less than the total domain transit time t_p, a second delay section is needed per stage. Two clocks of period t_c which are 180^o out of phase are used to drive half of each stage. To insure proper propagation and timing of the input signal through the shift register, $t_c = 2t_d > t_p$ must be fulfilled (Ref 5:927).

Using TELD device dimensions in Figure 28, two four terminal TELD AND gates were declared and connected as shown in Figure 32. No data was obtained as ASPEC failed to run

```
.PC BRIEF NP
.OP TRAN VOL
.CONTROL RMAX=.05
.OUTPUT -2.5 2.5 VC1 4 0 I*10 VANODE VOUT*.5 23 0
+ VG1*.5 13 0 VG2*.4 14 0
.MACRO TELD  0 1 3 4 12 13 14 23
VANODEP    2     0 DC 0 PL 0/0 0/1PS 46.75/2PS
RO         2     1    2659.33K
CO         1     0    .03PF
SO         1     5    3    0       2V   NC 1GG       4999
SOLL       1     6    1    0    2.10V   NC 1GG       1
SOVG1      5    15    13   0   -3.99V   NO 1         1GG
SOVG2      15    0    14   0   -3.99V   NO 1         1GG
SOVGP1     1     6    13   0   -3.99V   NC 1GG       1
SOVGP2     1     6    14   0   -3.99V   NC 1GG       1
BO         6     0    2.10V .1
R2         2     3    38.11K
C2         3     0    .03PF
S2         3     0    4    0       2V   NO 100       1GG
S2LL       3     7    3    0     2.1V   NC 1GG       1
B2         7     0    2.10V .1
R1         2     4    764.62K
C1         4     0    .03PF
S1         4     8    1    0       2V   NO 99        1GG
S1D        8     0    4    0       2V   NC 1         901
S1LL       4    10    4    0     2.1V   NC 1GG       1
S1VSUS     4    10   12    0   46.00V   NC 1         1GG
S1VG1      4     9   13    0   -3.99V   NC 1GG       1
S1VG2      4     9   14    0   -3.99V   NC 1GG       1
S1C        9    10    1    0    1.99V   NO 1         1GG
B1         10    0   2.10V .1
ST1        12   11    1    0       2V   NO .1        560
ST2        12   11    4    0       2V   NC 1GG.      .1
STVSUS     12   11   12    0   46.00V   NO 1         1GG
RI         11    0   305
RX         13    0   1G
RX1        14    0   1G
RX2        23    0   10K
VGOUT      20    0   0 DC 0 PL 0/0 0/1PS -4.01/2PS
SVCO       20   21    1    0       2V   NC 1GG       1
SV1X2      21   22    4    0    1.98V   NO 1         1GG
SV1X1      22   23    4    0    1.78V   NO 1GG       13
.EOM
XTELD 0 1 3 4 12 13 14 23 TELD
VANODE   12 0 DC 0 PL 0/0 0/1PS 46.75/2PS
VGATE1   13 0 DC 0 PL 0/0 0/10PS -4/10.01PS -4/100PS
VGATE2   14 0 DC 0 PL 0/0 0/30PS -4/30.01PS -4/100PS
.END
```

Figure 30. Four Terminal AND Gate data for ASPEC.

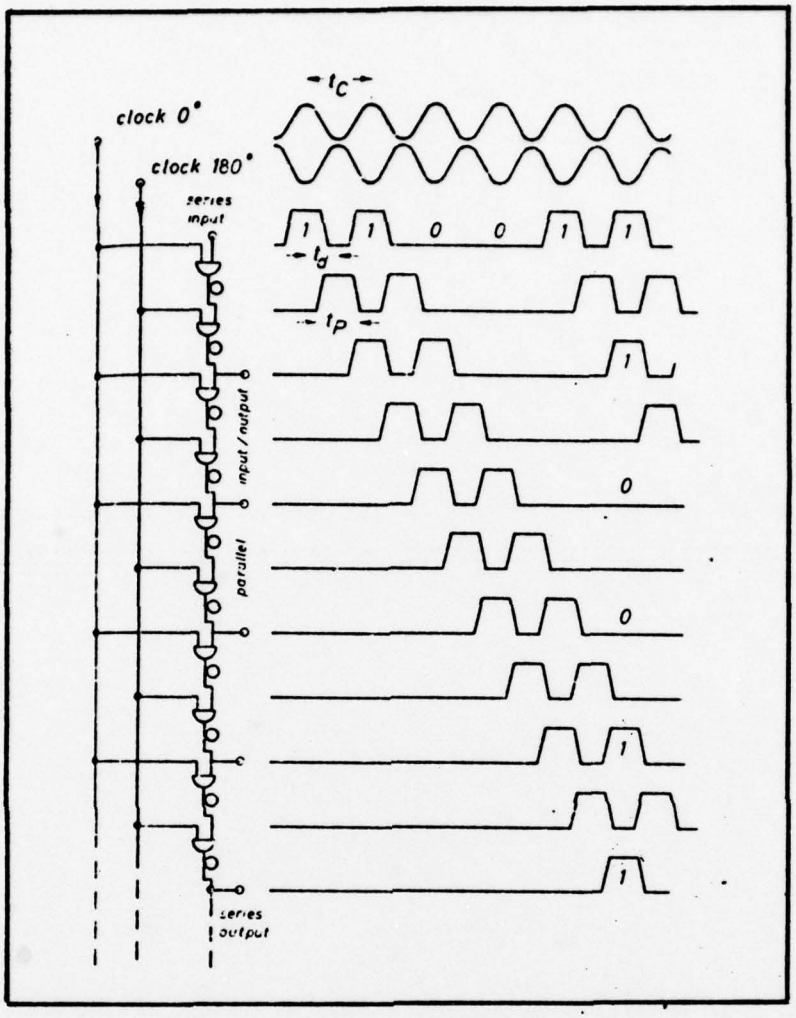


Figure 31. Dynamic shift register proposed by Mause (Ref 5:927).

because element count limitations were exceeded. A short discussion of the limitations encountered during TELD simulation using ASPEC can be found in section IV.

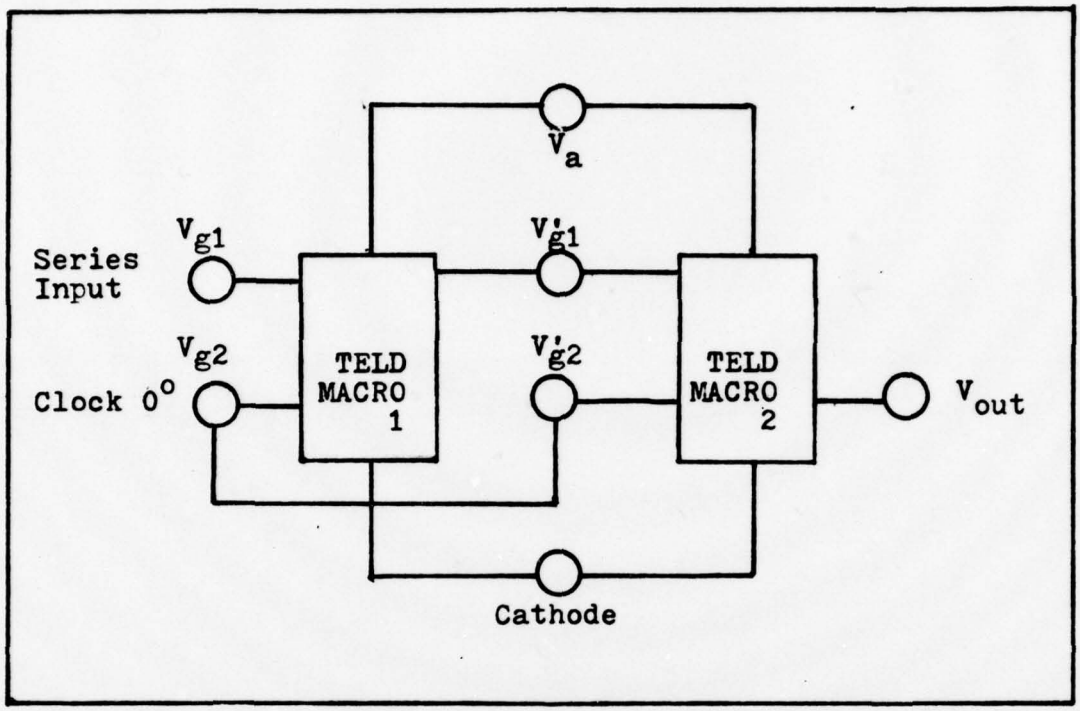


Figure 32. First stage of a dynamic shift register.

IV Conclusions

Introduction

The purpose of this thesis was to simulate TELD characteristics in order that the model might be used as a tool to devise some basic rules for design of logic circuits using TELDs. Because this is a first attempt to model TELDS for circuit operation, it was not expected that a definitive model would be the final result. However, it is believed that the work accomplished is a useful beginning step in the development of TELD circuit models and the study of logic operations using these models. This section will discuss conclusions that may be reached from these results in the areas of model weaknesses and strengths, problems encountered using ASPEC, and logic function considerations.

Model Evaluation

To evaluate a circuit model of a device two important areas must be considered. First, how closely does it reflect actual device operation and how accurately does it reproduce device output stimulated by certain inputs? Second, how convenient is the model to use?

Weaknesses. Although the model that has been derived does reflect the basic concept of TELD operation, it has two deviations from the discharging action of domain capacitance. First, it is apparent from the circuit model that the domain capacitance was not charged and discharged through a resistance equal to the crystal resistance. It was necessary to

use large resistor values and consider domain charging complete at values less than the actual estimate in order to insure minimum cross interference between the separate stages of the TELD oscillator circuit and to simulate domain propagation time. Second, the reduction of crystal charging resistance due to domain spreading during the growth cycle was not duplicated. For devices with long active channels and small domain lengths, this effect is not significant, as in the case of the device of Table I. If the active channel length is small and a significant portion is consumed by the domain, the change of the charging resistance of the domain can produce significant changes in device operation.

Another deviation from actual device operation is the method used to duplicate propagation of the domain. Ideally a TELD circuit model should have a domain capacitor that is charged through crystal resistance and maintains that charge for some time equal to the propagation time of the mature domain to the anode where it can be discharged. The circuit model used required separate RC circuits for charging, propagation, and discharging of the domain. This increased element count significantly and limited the use of the model to single basic gates for each computer run.

Strengths. The accuracy of the model appears to be limited only by the accuracy of the device parameters used. If T_{df}, T_{wd}, T_{de}, and ΔI as defined in section III are known for a particular device, the only limit on accuracy is general shape of the output pulses. Output for the circuit

model is a square pulse. It is apparent from the circuit model that internal resistance and capacitance values may be adjusted to obtain exact results. In general, the accuracy of the model is only limited by the computer time-step used for simulation which is discussed later.

A circuit model must also be convenient if it is to be a useful tool in design. Although no formalized procedure has been provided for the use of the circuit model presented in this paper, the use of the model seems straightforward and has not proven difficult to use. All equations require simple computation and it is possible to make reasonable guesses for element values if the model operation is understood.

Overall Evaluation. There are two areas where the model has weaknesses which suggest that other approaches should be investigated. First, the model is not consistently analogous with device physics as previously discussed. Second, as demonstrated by the attempt to simulate a shift register, the element count is so high as to prevent the use of this model with ASPEC. It was impossible to simulate two AND gates of the shift register, and unless ASPEC is changed, simulation of logic functions using this model is limited to the use of one gate. It should be pointed out, however, that simulation of the simple AND and OR gates has provided useful information about logic operations with TELDs which is discussed in this paper.

Evaluation of the Use of ASPEC for Circuit Modeling of TELDs

The approach used for modeling of TELDs was dictated by the fact that there appeared to be no other choices available given the list of ASPEC circuit elements and the time to produce a working model. Once work began ASPEC proved to be a very useful tool.

Problems. One problem that occurred which cannot be avoided in any circuit analysis program is that increased accuracy (decreased time-step) required increased CPU time. Any variation in the requested transient response time produced a variation in output even though circuit elements did not change. In order to get accuracy in the picosecond range it was not necessary to reduce the time-step used by ASPEC. The ensuing result was that simulation of devices with long channel lengths produced excessive CPU time and often exceeded disk storage. The solution was to simulate devices with shorter channel lengths and accept reduced accuracy.

Limitations on element count proved to be a significant problem in the simulation. It is unknown at this time what the implications of increasing the element count are, but if other approaches to modeling TELD logic gates prove unsuccessful, it is suggested that the element count limit be increased.

Overall Evaluation. The problems encountered using ASPEC were primarily a function of the circuit model devised for TELDS. In general ASPEC is an extremely flexible program

and it is recommended that any future attempts at modeling TELDs use ASPEC. Other more efficient approaches may not encounter the same problems found in this approach using ASPEC.

Logic Function Considerations

Although it proved possible to simulate only AND and OR gates, several important points about the use of TELDs as logic gates are apparent.

The first point is that logic operation speed is a direct function of domain formation and, or, propagation time for all types of TELDs (two, three, and four terminal devices). Two and three terminal devices would appear to produce the shortest time delay as they can output a voltage pulse (to be summed with a bias voltage to trigger another TELD) as soon as the domain has formed whereas four terminal time delay is increased by the time required for the domain to propagate to an electrode for triggering other devices. For short devices the four terminal TELD may be faster because of the additional charging time of the domain capacitance incurred when a series resistor is added to produce a voltage output pulse in two and three terminal operation. This is an area that should be investigated further when an acceptable TELD model is derived.

Second, noise is always an important consideration in logic operation with real devices. In the discussion on three terminal OR operation it was noted that the total on time (see Figure 24) of both gates must be greater than T_{df}

where the first pulse to arrive begins domain formation. Should a noise pulse of sufficient magnitude arrive at one gate shortly before the arrival of a signal pulse at another gate such that they overlap in time as shown in Figure 24 (V'_{g1} is the noise pulse), the output signal will appear sooner at the output terminal because the domain began to form when the noise pulse triggered it. If there is a gap in time between the signal and the noise pulse such that they do not overlap, there will be a delay at the output terminal by the length of the noise pulse minus the time gap because the noise pulse created a partial domain that must be extinguished before another may form. If the partial domain is large and the signal pulse is short, there may be no output as extinction of the partial domain may overlap the input signal in time such that there is not enough time remaining on the signal pulse at the end of partial domain extinction time to sufficiently trigger a mature domain. AND gate operation does not appear to be susceptible to noise in the same manner as OR gate operation because no partial domain can form until both gates are properly biased.

One serious implication of logic operation with TELDs is that there appears to be no inverting capability in the conventional sense. A conventional inverter maintains the output state opposite to the input state for as long as the input state is applied and can be triggered by either a positive or negative going pulse. A TELD is a leading edge triggered device that produces an output whose length is

basically independent of the input pulse width. The output state will, therefore, not be maintained opposite the input state for the duration of the input pulse. A TELD may be triggered by either a positive or a negative going pulse depending on the configuration, but not both. Further investigation into configurations for TELD inverters should be made if more complex functions are to be realized.

General Observations

It seems apparent from data obtained during the literature search and circuit modeling that TELDs have great potential for high speed logic operations. It is also apparent that practically every area of study concerning TELDs is in its first stages and much work needs to be done. In the area of logic operation, no definitive rules or methodologies have been proposed. It seems important, therefore, that a good model be developed that may be used to explore possible TELD logic fundamentals. Section V sets forth some specific recommendations that seem appropriate for the next steps beyond the work accomplished for this thesis.

V Recommendations

Model Approach Proposal

Several models were proposed in section II of this paper and it was stated that a FET model with a time varying transconductance might prove to be an appropriate model for a TELD. This approach is suggested for the following reasons. First, a TELD and a FET are constructed in much the same way. Both have an anode, a cathode, a channel, and a gate under which depletion of the channel controls the operation of the particular device. Second, transconductance is an ideal way to simulate the current changes through a TELD because of domain action. This requires that the transconductance be time varying as a function of domain formation, propagation, and extinction as well as gate voltage.

To approach this modeling effort, it would be necessary to obtain a complete copy of the ASPEC program. From information obtained therein it may be possible to alter the library FET model to include a gate triggered time varying transconductance where the frequency and pulse width would be determined by domain characteristics. It would also be necessary to add elements to represent the capacitive electrode. A problem that may occur here is obtaining proper electrode polarity for triggering follow-on TELDs. The advantages of such a model could be more realistic simulation of gate electrode operation, reduced CPU time, and simulation of large devices using TELDs because FET device count limitation for ASPEC is 100 whereas the count

limitation for macros is only 10.

Proposed Areas of Study

Once an efficient model of a TELD is devised, there are several areas of logic operation that should be investigated. If more complex logic functions than AND and OR gates are to be available using TELDs, it is important that some form of invert function be devised. One possible approach would be to place a load resistor (equal to R_o) at the cathode of, and in series with, a two terminal TELD. The anode would be biased positively and the load resistor, negatively such that the cathode of the TELD would be at ground. The anode bias should maintain the TELD internal field below E_{sus} and be pulsed above threshold when inverting is required. Thus, the output voltage (taken at the TELD cathode) would go negative when the anode voltage goes above threshold. To insure that the output voltage returns to ground when the input pulse drops requires that the entire invert take place in less than one cycle. The return of the anode voltage to a point where the internal E field is below E_{sus} while the domain is propagating would cause the domain to decay and the internal resistance to decrease to R_o. If the input anode pulse drops after the domain extinguished itself, no actual invert operation can take place as the input pulse does not exercise control over the domain propagation by returning the cathode to ground.

One other area of study might be the logic implications of intermixing two, three, and four terminal TELDs. Two

terminal TELDs are triggered by a positive pulse applied at the anode whereas three and four terminal TELDs in the depletion mode are triggered by negative going pulses. It may be possible to construct complex logic functions with two, three, and four terminal TELDs that realize advantages in triggering logic and speed.

Summary

The TELD circuit modeling accomplished using ASPEC has proven useful and informative. It has demonstrated AND and OR capability but indicated the need for a more efficient model. It also pointed out the difficulties in obtaining an inverter and the logic implications of such a device using TELDs. It is hoped that the proposals for another model and areas of study will be helpful to anyone interested in devising a TELD circuit model.

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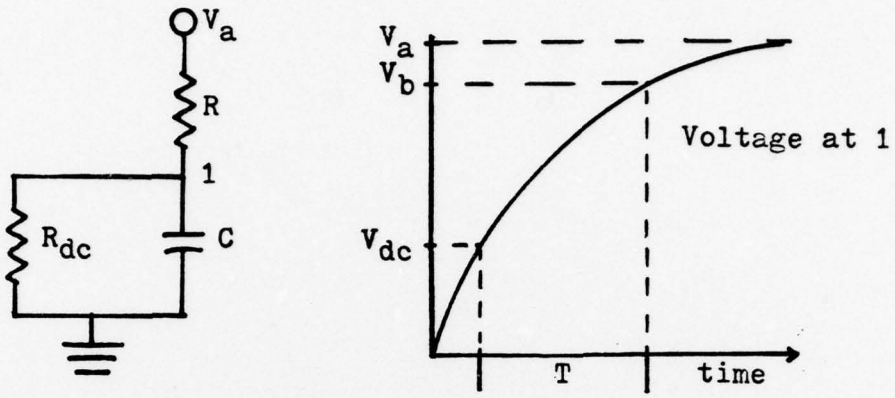
Appendix: Recursive Solution for R



$$R_{05} = T_{04}/C_{03}\ln[(V_{a00} - V_{b01})/(V_{a00} - V_{dc02})]$$

$$V_{dc02} = V_{a00}[(V_{a00}R_{dc06})/(R_{05} + R_{dc06})]$$

$$V_{dc02} - [1 + (\Delta V_{08}/V_{dc02})]V_{dc02}$$

This program solves for R_{05} (subscripts indicate the TI 59 data register used) as described in section III when all other variables are known. Zero is considered to be 10^{-6} unless another value is defined.

Procedure

1. Load Data
   - Reg(00) - V_a
   - Reg(01) - V_b
   - Reg(02) - Guess, V_{dc}
   - Reg(03) - C
   - Reg(04) - T
   - Reg(06) - R_{dc}
2. Execute
   Press A
   EOP, R - display
3. Iteration Count
   Press C
4. User defined 0
   Dsp., Press 2nd A'

Program

LOC	CODE	KEY	LOC	CODE	KEY	LOC	CODE	KEY
00	76	*Lbl	34	03	03	68	50	*1X1
01	11	A	35	95	=	69	22	INV
02	93	.	36	35	1/X	70	77	*x≥t
03	00	0	37	65	X	71	12	B
04	00	0	38	43	RCL	72	53	(
05	00	0	39	04	04	73	43	RCL
06	00	0	40	95	=	74	08	08
07	00	0	41	42	STO	75	55	/
08	01	1	42	05	05	76	43	RCL
09	76	*Lbl	43	85	+	77	02	02
10	16	A'	44	43	RCL	78	85	+
11	42	STO	45	06	06	79	01	1
12	10	10	46	95	=	80	54	)
13	76	*Lbl	47	35	1/X	81	65	X
14	17	B'	48	65	X	82	43	RCL
15	43	RCL	49	43	RCL	83	02	02
16	00	00	50	06	06	84	95	=
17	75	-	51	65	X	85	42	STO
18	43	RCL	52	43	RCL	86	02	02
19	01	01	53	00	00	87	69	*OP
20	95	=	54	95	=	88	29	29
21	55	/	55	42	STO	89	61	GTO
22	53	(	56	07	07	90	17	B'
23	43	RCL	57	75	-	91	76	*Lbl
24	00	00	58	43	RCL	92	12	B
25	75	-	59	02	02	93	52	EE
26	43	RCL	60	95	=	94	43	RCL
27	02	02	61	42	STO	95	05	05
28	54	)	62	08	08	96	91	R/S
29	95	=	63	43	RCL	97	76	*Lbl
30	23	ln	64	10	10	98	13	C
31	94	+/-	65	32	x≷t	99	43	RCL
32	65	X	66	43	RCL	100	09	09
33	43	RCL	67	08	08	101	91	R/S

Note that "/" is used for "divide by."

VITA

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Circuit Model

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The operational characteristics of Transferred Electron Logic Devices (TELDs) were summarized and used to devise a circuit model for simulation of basic logic gates. The model consists of an oscillator and a voltage controlled switch. The oscillator is a series of RC circuits that discharge at rates proportional to the TELD domain formation, propagation, and extinction times. The switch is controlled by the oscillator and simulates the internal increase of device resistance due to electron transfer to states

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of decreased mobility under high field conditions. The model successfully simulated three and four terminal AND and OR gate operations and demonstrated the need for special considerations to be taken when logic operations with TELDs are performed.